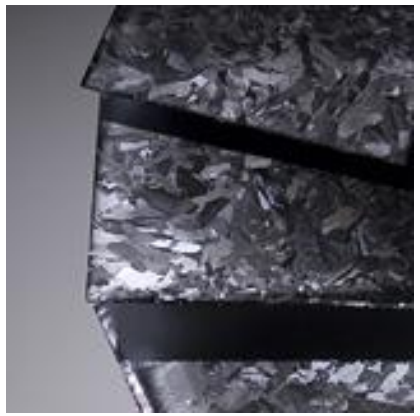
Fundamentals and processes for photovoltaic devices

Chapter IX.

Silicon material and wafer preparation



Lecture Outline

1. Crystalline Si standard chain
2. Generality
3. Metallurgical grade (MG)
4. Purification via the gas phase Siemens process
5. Ingot fabrication
6. Wafering and grey energy
7. Mechanical properties of silicon
8. Material and energy for wafer
9. Alternative approach to wafering

1. Crystalline silicon standard chain

1. Solar grade Si → 2. Ingot → 3. Wafering → 4. Cell process → 5. Module

2. Ingot: mono, multi

2. Generality

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Wafers are keys

1. Material quality (can allow or not high efficiency with good lifetime)
2. Costs component (mostly the polysilicon)
3. Strong impact on grey energy and CO2 equivalent emission

E.G in 2000, around 20 g of silicon per Watt of module and 250 kWh/kg of silicon → 5 kWh of energy for the silicon
5 years energy pay-back time for Si (at 1kWh/W per year)

1. Crystalline silicon standard chain

In 2024 a high quality mono-crystalline wafer costs

- 3 cts/W to produce
- or 30 cts for a 182x182 mm2 Wafer….
- or 6 $/m2 !!

It is typically

110 microns thick for a silicon heterojunction
130 micron thick for a Topcon solar cell
150 micron thick for a PERC solar

The higher the final cell efficiency, the higher the required lifetime and the highest the silicon quality !

1. Crystalline silicon standard chain

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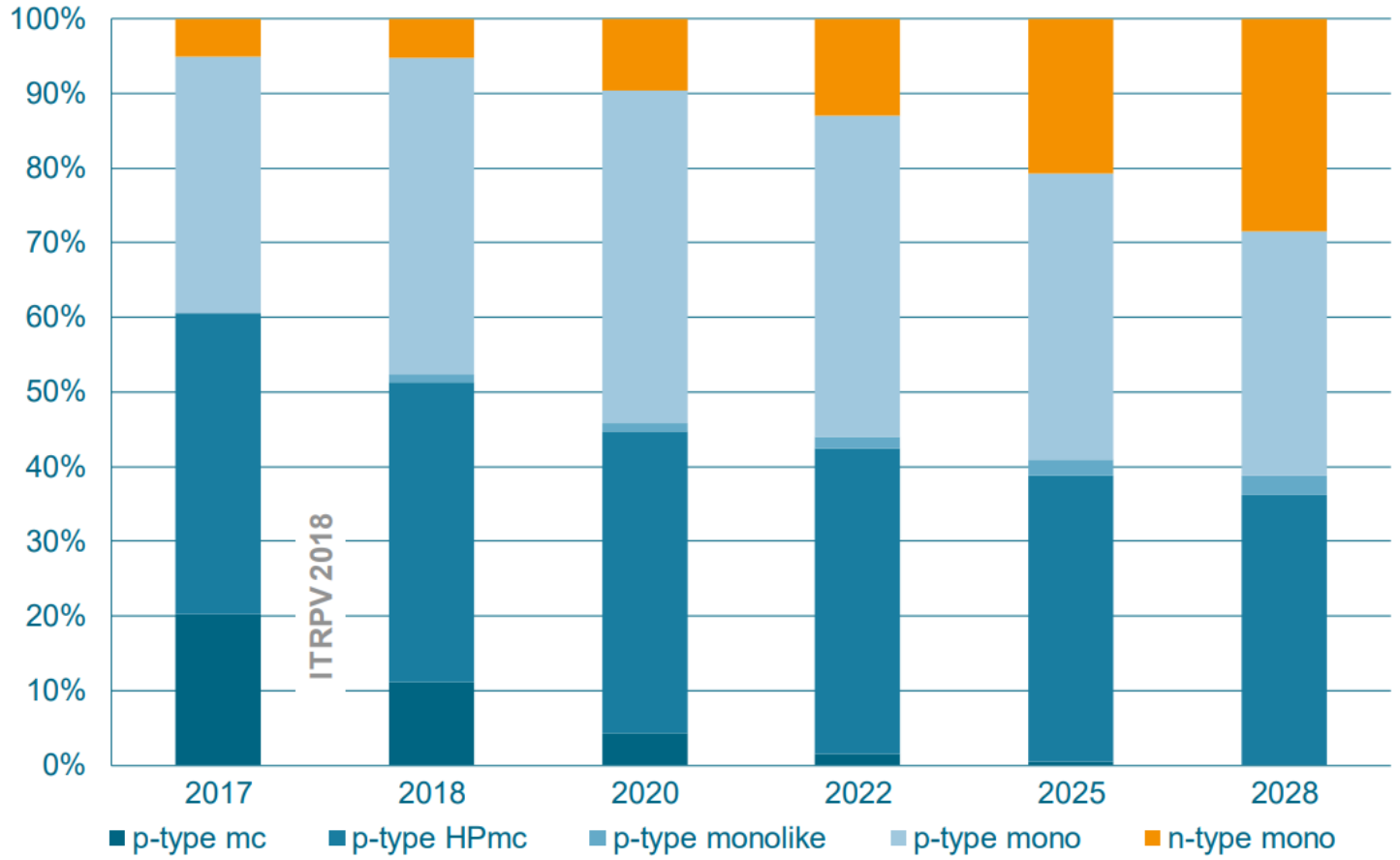
Different wafer types

World market share [%]

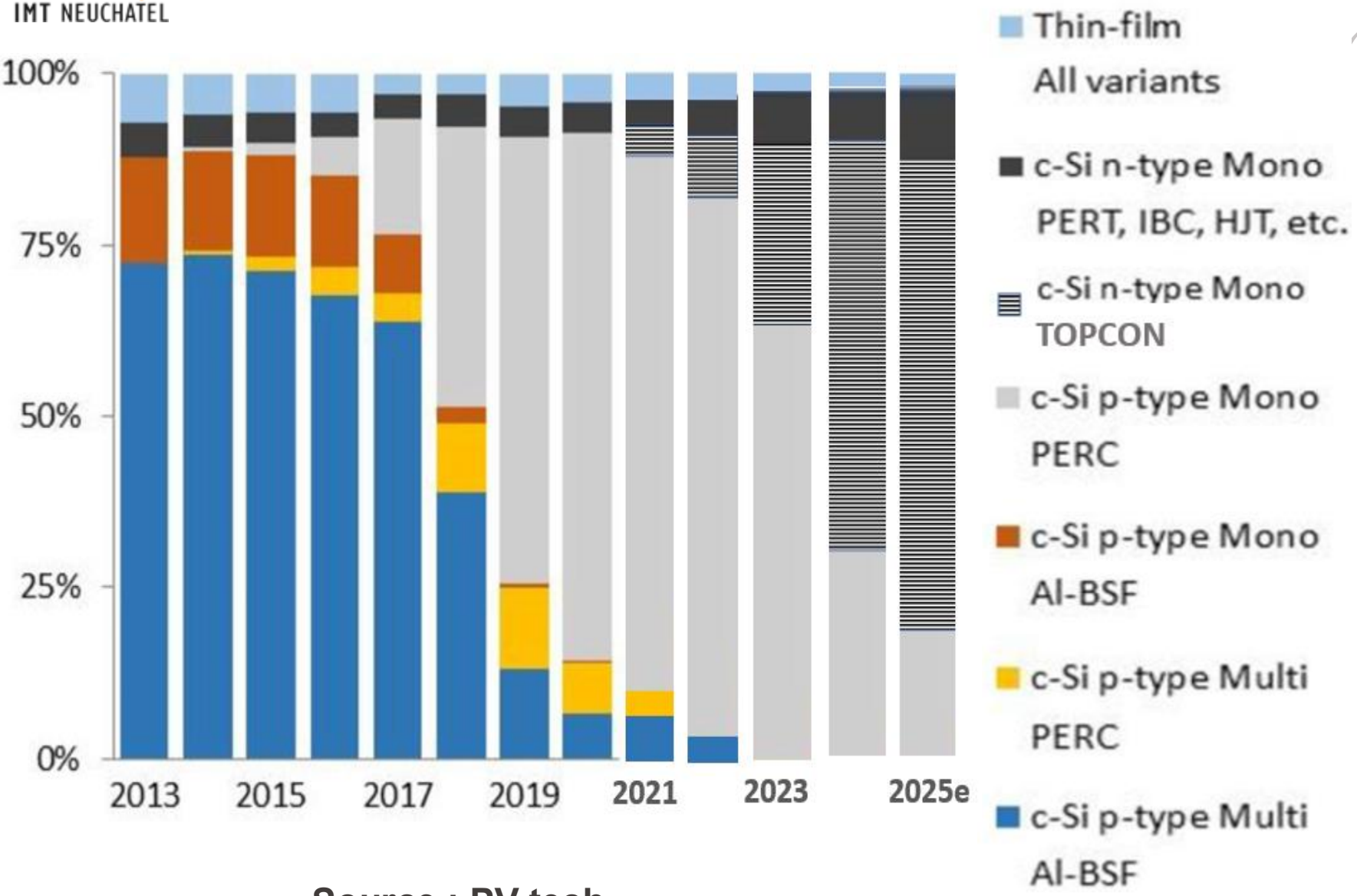


In 2018 the industry predicted that Multi would still occupy over 80% of the market in 2025

Multicrystalline

High performance multicrystalline

Reminder: Drastic changes in the PV industry



Source : PV tech

2015-2020 shift from multi to monocrystalline silicon

Thanks to progress in «crystal pulling and sawing», and high efficiency cell process

2017-2021 Shift from Al-BSF cell to PERC solar cells were taking 85% of the market in 2020

TOPCON (Mostly) and Heterojunction SOLAR CELLS will replace PERC solar cells (2023-2027). No mc-Si in 2025 anymore

2. Generality

Wafers for microelectronics and photovoltaics

The preparation is the same and consists of **the following steps**:

1. Solar grade Si
   - preparation of metallurgical grade (MG) Si
   - purification via gas phase
   - fabrication of (electronic grade) polycrystalline Si rods or granules
2. Ingot
   - growth of single crystals with Czochralski (Cz) or float-zone (FZ) growth or multicrystalline ingots (or quasi-mono)
3. Wafering
   - cutting into wafers

Multicrystalline (mc) Si

Monocrystalline c-Si

1. Crystalline silicon standard chain

In 2024 a high quality mono-crystalline wafer costs

- 3-4 cts/W to produce in China
- or 30 cts for a 182x182 mm2 Wafer….
- or 6-8 $/m2 !!

It is typically

110 microns thick for a silicon heterojunction
130 micron thick for a Topcon solar cell
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The higher the final cell efficiency, the higher
The lifetime and the highest the silicon quality !

2. Generality

Solar grade polysilicon

target

1. Solar grade Si

Reminder: 1 ppbw (part be billion weight) in Fe inside a wafer can lead to a low lifetime (microsecond range) and reduce efficiency dramatically

Poly Silicon specification			
	µE grade	solar grade	
		for mono cells	for multi cells
Donor [ppba]	< 0.1	< 0.5	< 5
Acceptor [ppba]	< 0.03	< 0.1	< 0.5
Carbon [ppma]	< 0.1	< 0.5	< 0.5
Total heavy metal [ppbw]	< 0.5	< 15	< 15

Goal:
Less than ppba (part per billion) dopants, less than ppbw (ppb weight) of heavy metal impurities

If more iron (e.g. 10 ppbw) is present in the polysilicon, part of it can be segregated during ingot and cell processing (gettering)… but more is dangereous!

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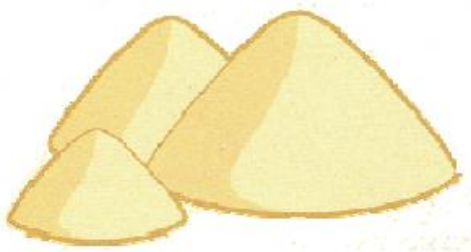
3. Metallurgical grade Si (MG):

First step

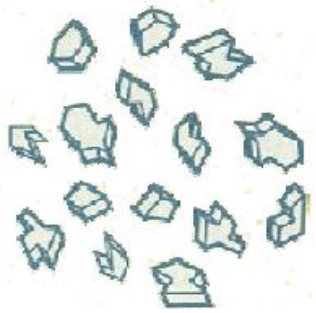
Preparation of metallurgical grade (MG) Si

- Reduction of quartz sand (SiO_2, widely available) with graphite (C) (and some wood chips) in an arc furnace at high temperatures.



quartz sand
or quartzite

$$SiO_2 + 2C \xrightarrow[14\,kWh/kg\,Si]{1800\,^\circ C} Si + 2CO$$



Typ 99 % pure
metallurgical Si
1% impurities and hence
improper for solar cells

3. Metallurgical grade Si (MG):

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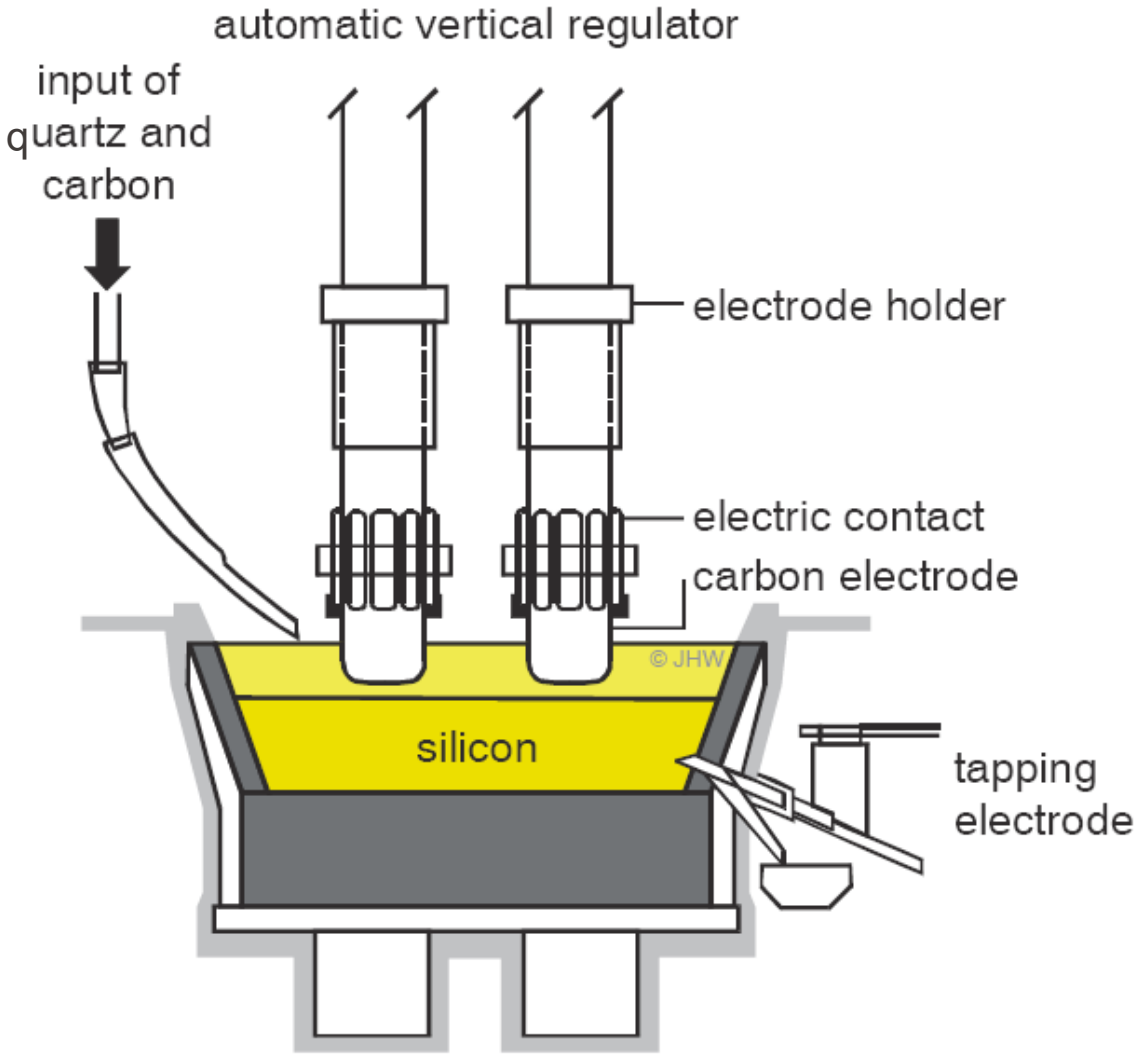
Arc furnace for metallurgical grade Si (MG)



- Continuous mode arc furnace preparation of metallurgical Si.
- Electrical current passed between the carbon contacts heats the melt.
- The silicon dioxide (quartz sand) reacts with carbon and forms metallic liquid Si (melting point 1415 °C) as well as carbon monoxide.
- Quartz sand and carbon are continuously fed into the vessel.
- Requires around 12-14 kWh/kg of Si
- Typical 1-2$ manufacturing costs

The Production Of Silicon | NTNU - YouTube

4. Purification of MG Si

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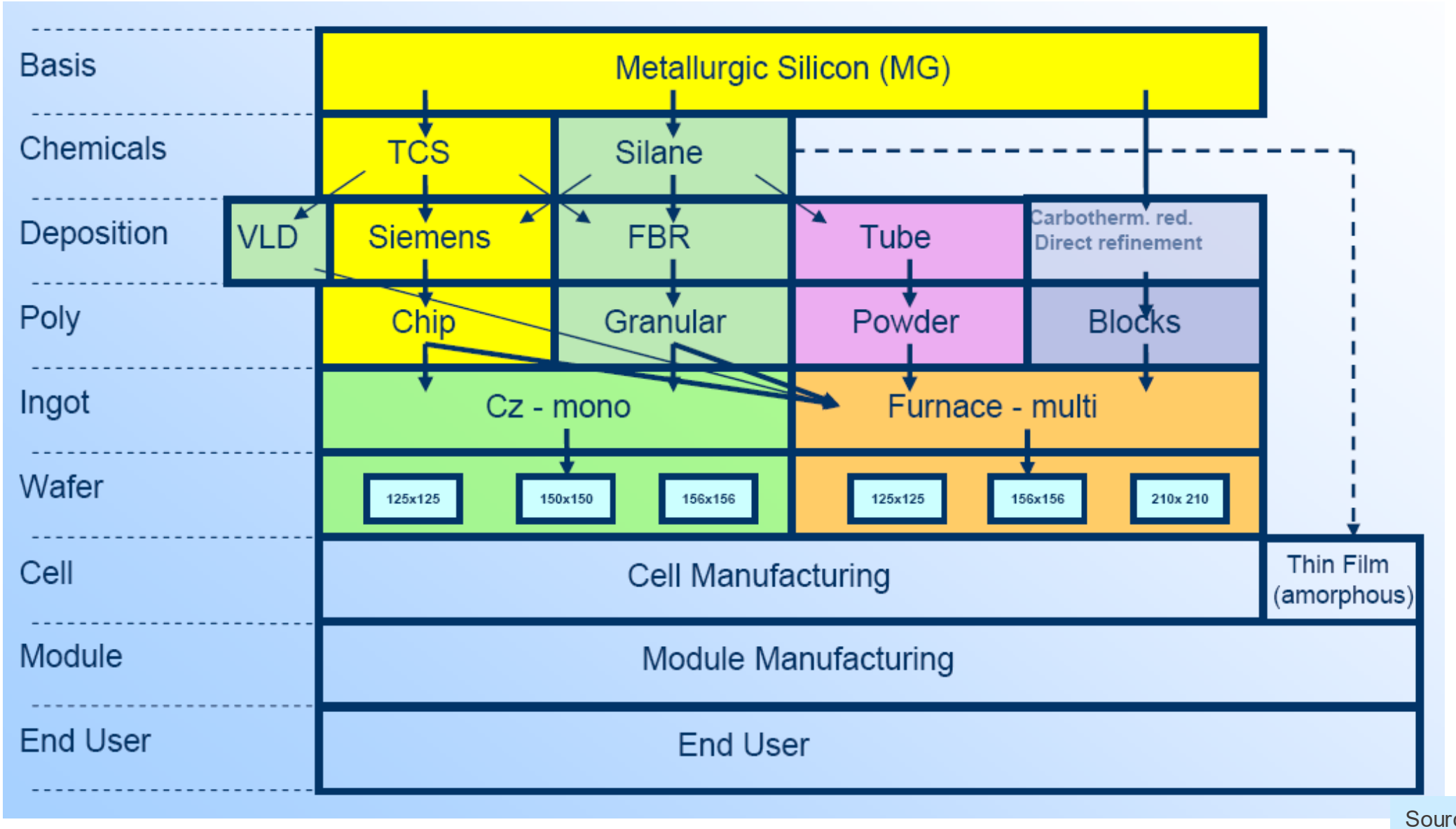
From MG grade Si to solar (or quasi-electronic grade)

- **Siemens process route with Tricholorosilane (TCS)**
- **Fluidized bed reactor route with silane**
- Direct metallurgical silicon refinement (but lower purity)

4. Purification of MG Si



Source
Fath, Centrotherm

4. Purification of MG Si

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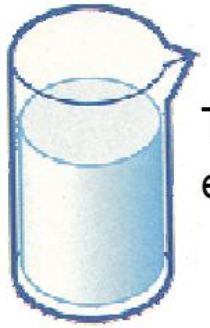
Purification via the gas phase

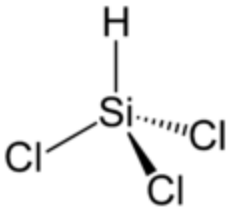
Cleaning of metallurgical Si is performed by repeated distillation via the gas phase. After making powder from the Si pieces, the Si is reacted with hot hydrochloric acid (HCl) to form liquid trichlorosilane.

Heavy metallic impurities (Fe, Ni, Cu etc.) which are solved in the $SiHCl_3$ have a lower volatility than the liquid itself.

$$Si + 3HCl \xrightarrow[\text{exotherm}]{300-400\,^{\circ}C} SiHCl_3 + H_2$$



Trichlorsilane evaporates at 30 °C



Trichlorosilane or TCS ($SiHCl_3$), liquid at 300 K

+

Purification by repeated distillation (3-7 times)

Highly pure TCS

4. Purification of MG Si

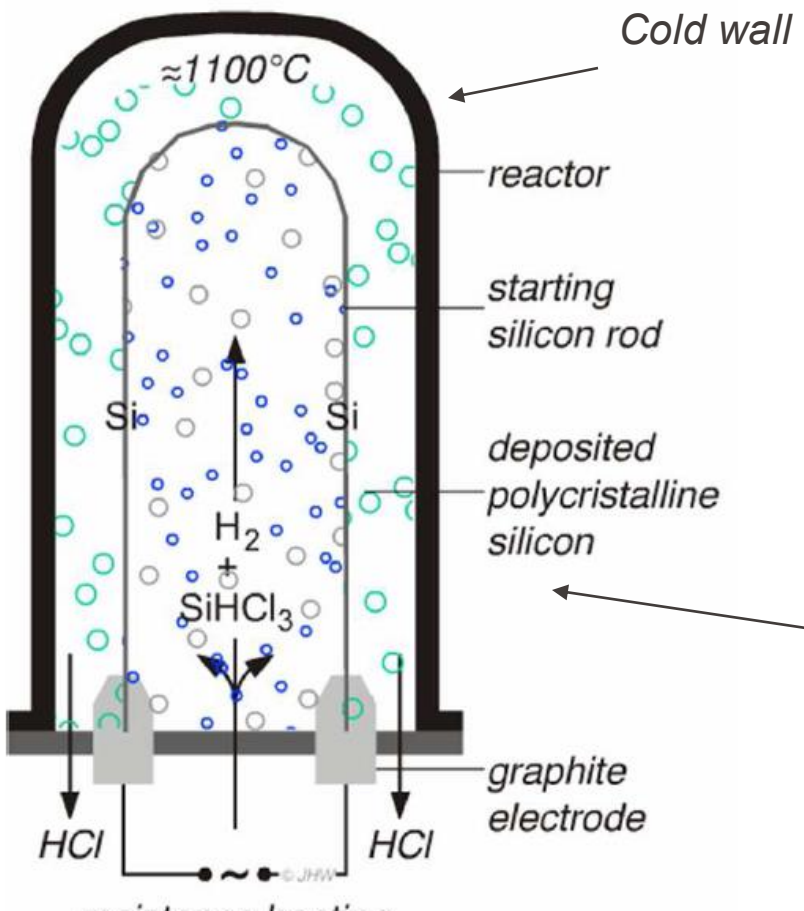
Trichloro-silane distillation

Tongwei's new 30,000-ton polysilicon plant in Baotou, Inner Mongolia came on stream in October 2018 – Image: Xinhua

4. Purification of MG Si: Siemens Process

In the **Siemens process**, high-purity silicon rods are electrically heated and exposed to trichlorosilane (TCS) at 1150 °C with additional H2. The TCS decomposes and deposits additional silicon onto the rods, enlarging them

$$4\,HSiCl_3 + 2H_2 \xrightarrow{1100°} 3Si + SiCl_4 + 8\,HCl$$



4. Purification of MG Si

Notes on Si purification

- The byproduct $SiCl_4$ (Silicon tetrachloride STC) can be partially reconverted to $HSiCl_3$ (STC-TCS converter → lower costs)
- Similar Siemens process exists with Silane instead of TCS
- Full Si process used to require a lot of energy (up to 200 kWh/kg of silicon in 2000)

- Use of larger reactor (up to 10 tonnes of silicon) and 72 filaments
- Use of reflected, coated Jars (less cooling)
- Use of tubular filaments (larger coating surface)

→ *Energy used down to 40-45kWh/kg*

EPFL

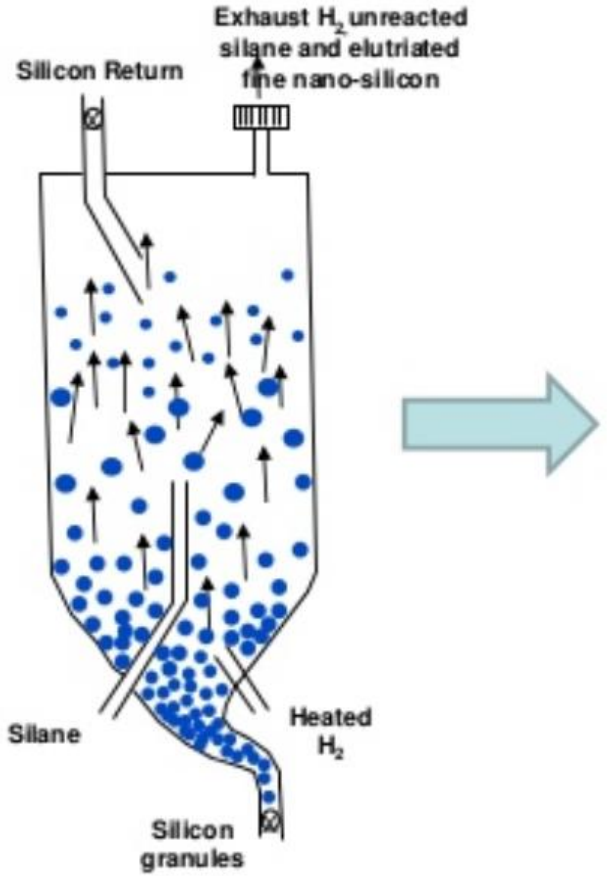
PV-lab
IMT NEUCHATEL

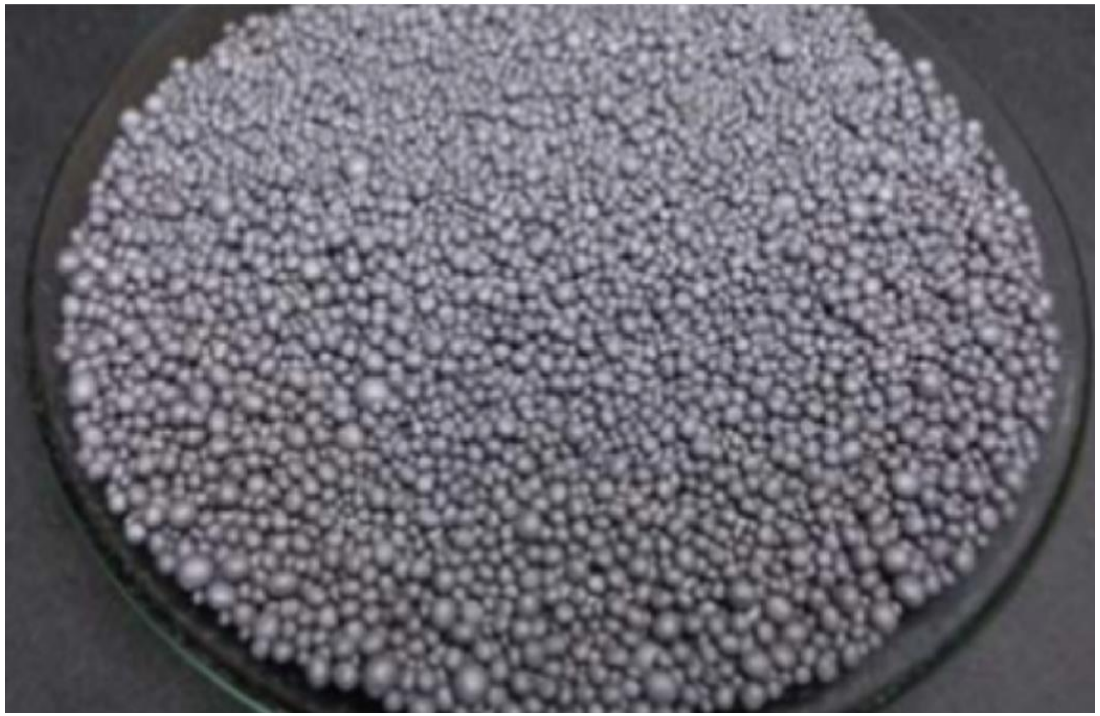
Advanced Material Solutions

4. Purification of MG Si

Fluidized bed reactor (still a small share of market)

Fluidized bed reactor (FBR), such as developed by REC or GCL, avoids the need for cold walls and could further reduce the energy consumption. Starting with silane (SiH4)
It produces small (mm size) Si granules





In 2021 GCL announced 20 kWh/kg for FBR process !

4. Purification of MG Si

Polysilicon capacity: in constant expansion

From 29'000 MT (metric tons) in 2004
To 620'000 MT (2021) to 1'200'000 MT in 2023 (enough for ~ 550 GW)

Status 2022

	The World's Top 10 Polysilicon Producers		
	Manufacturer	Country	Capacity
1	Tongwei	China	205,000
2	GCL Technology	China	140,000
3	Daqo New Energy	China	140,000
4	Wacker Chemie	Germany/USA	85,000
5	Xinte Energy	China	100,000
6	Xinjiang East Hope	China	70,000
7	OCI Company	South Korea/Malaysia	36,500
8	Asia Silicon (Qinghai)	China	52,000
9	Hemlock Semiconductor	USA	20,000
10	Shaanxi Non-Ferrous Tianhong REC Silicon	China	19,300
			Source: Bernreuter Research; Table: TaiyangNews

Capacity end 2023

345,000 MT
300,000 MT
240,000 MT

200,000 MT
130,000 MT

92,000 MT

2024: > 2 millions tons annual capacity
Enough for > 1000 GW of PV at 2 g/W

Source: www.bernreuter.com/polysilicon/manufacturers/

Polysilicon price: an history of bottleneck and oversupply

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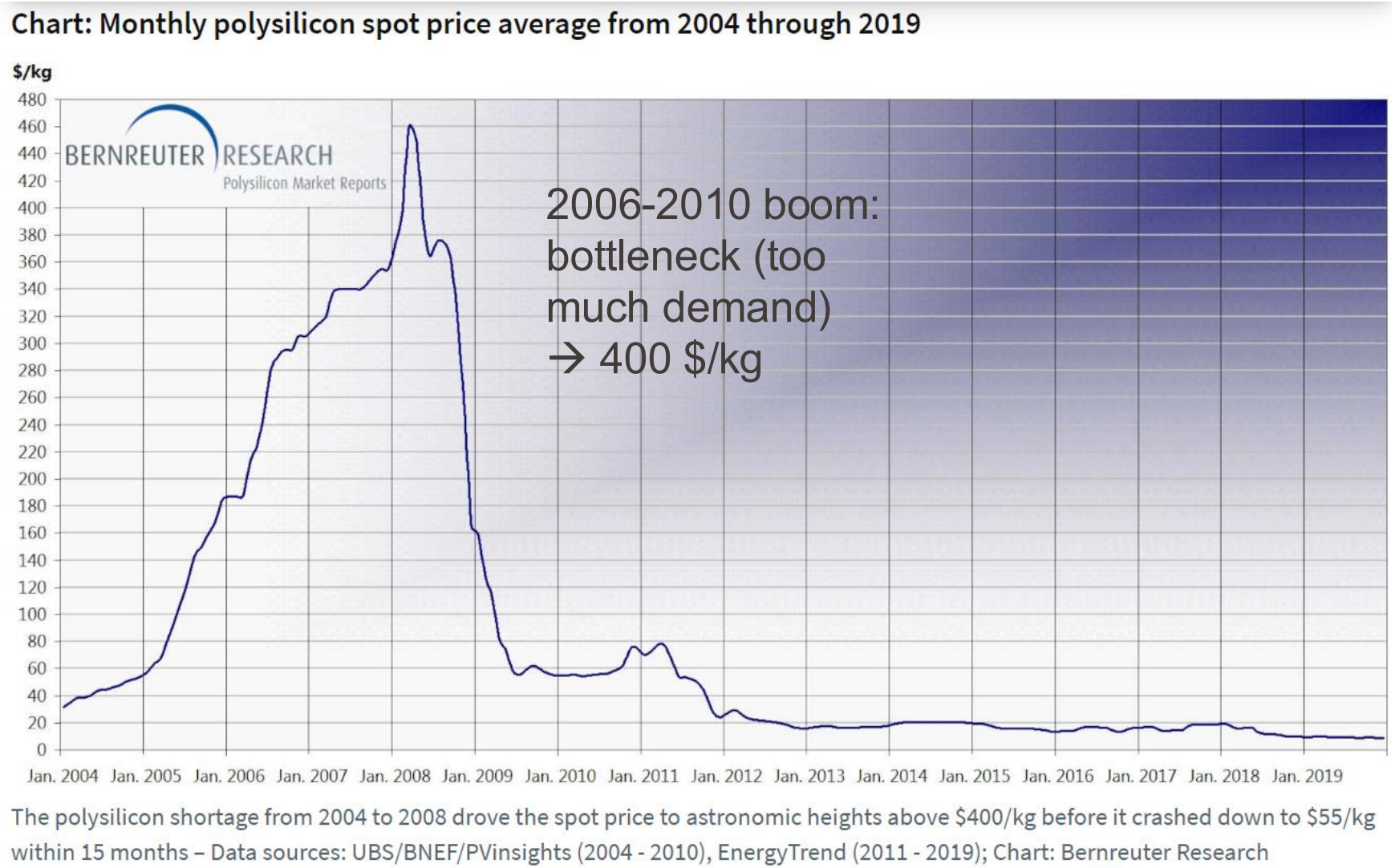
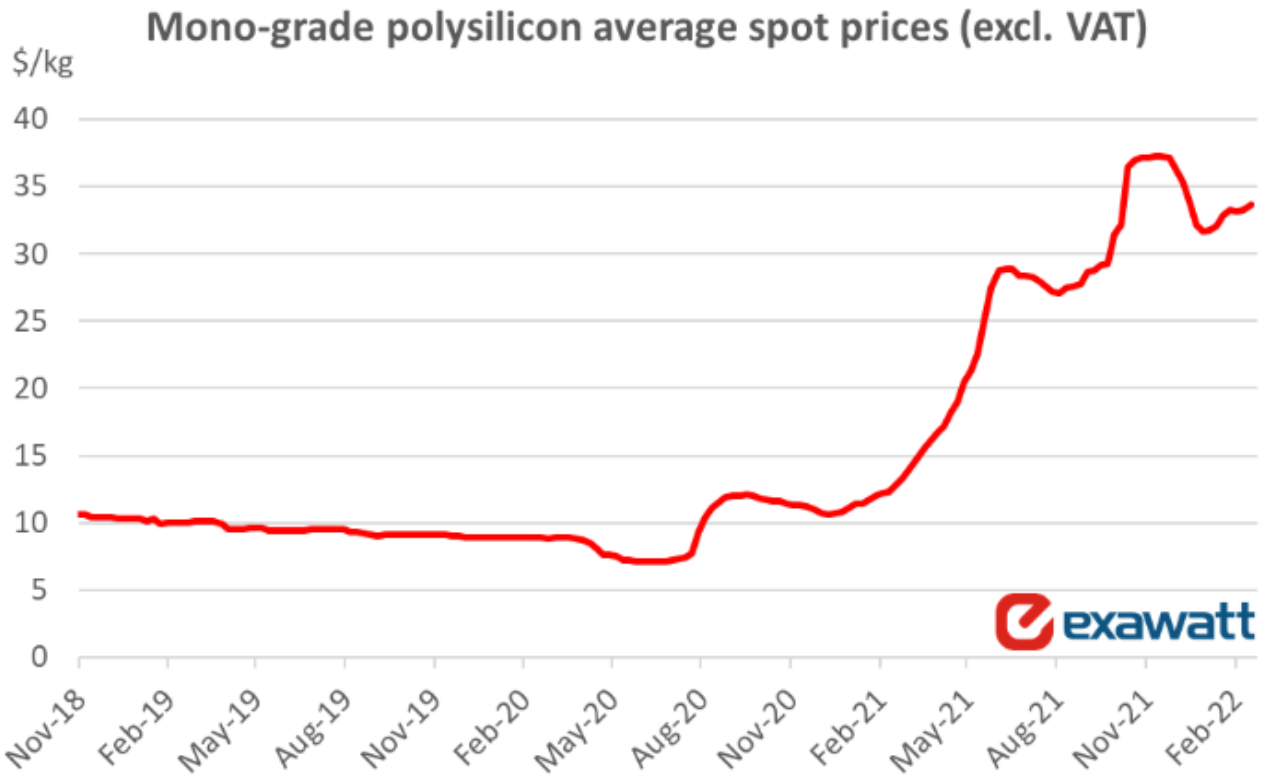


Then prices close to production costs in 2019-2020

- **Good quality polysilicon could be acquired at 10$/kg in 2020**
- High quality Wacker Silicon (Germany) 10-12$/kg

N.b. around 70 kWh/kg of Electricity for Si production
→ 3.5$/kg at 5cts/kWh.
Chinese companies have their Own coal powerplants.

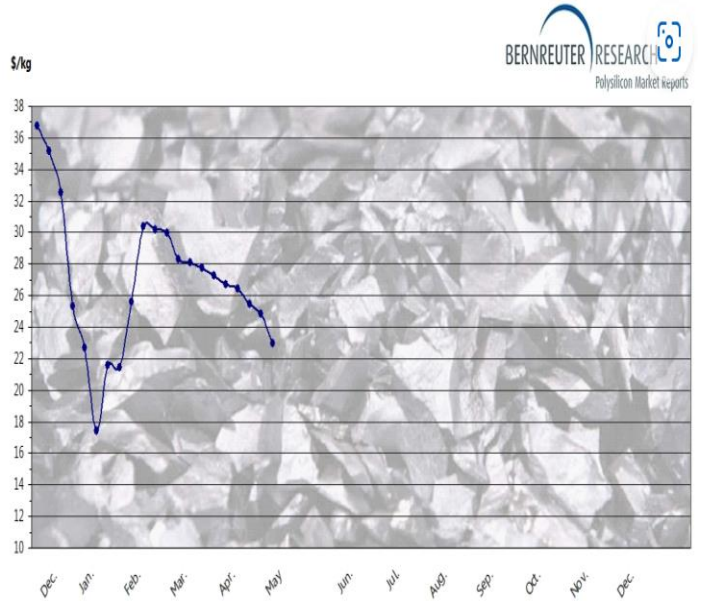
Strong price fluctuation



Polysilicon prices started to increase considerably in February 2021.

Source: Exawatt analysis of spot price data from China Nonferrous Metals Industry Association, EnergyTrend, PV InfoLink and PVInsights

Because
In 2022, all major polysilicon companies make huge profit.
They are upscaling massively the production capacity



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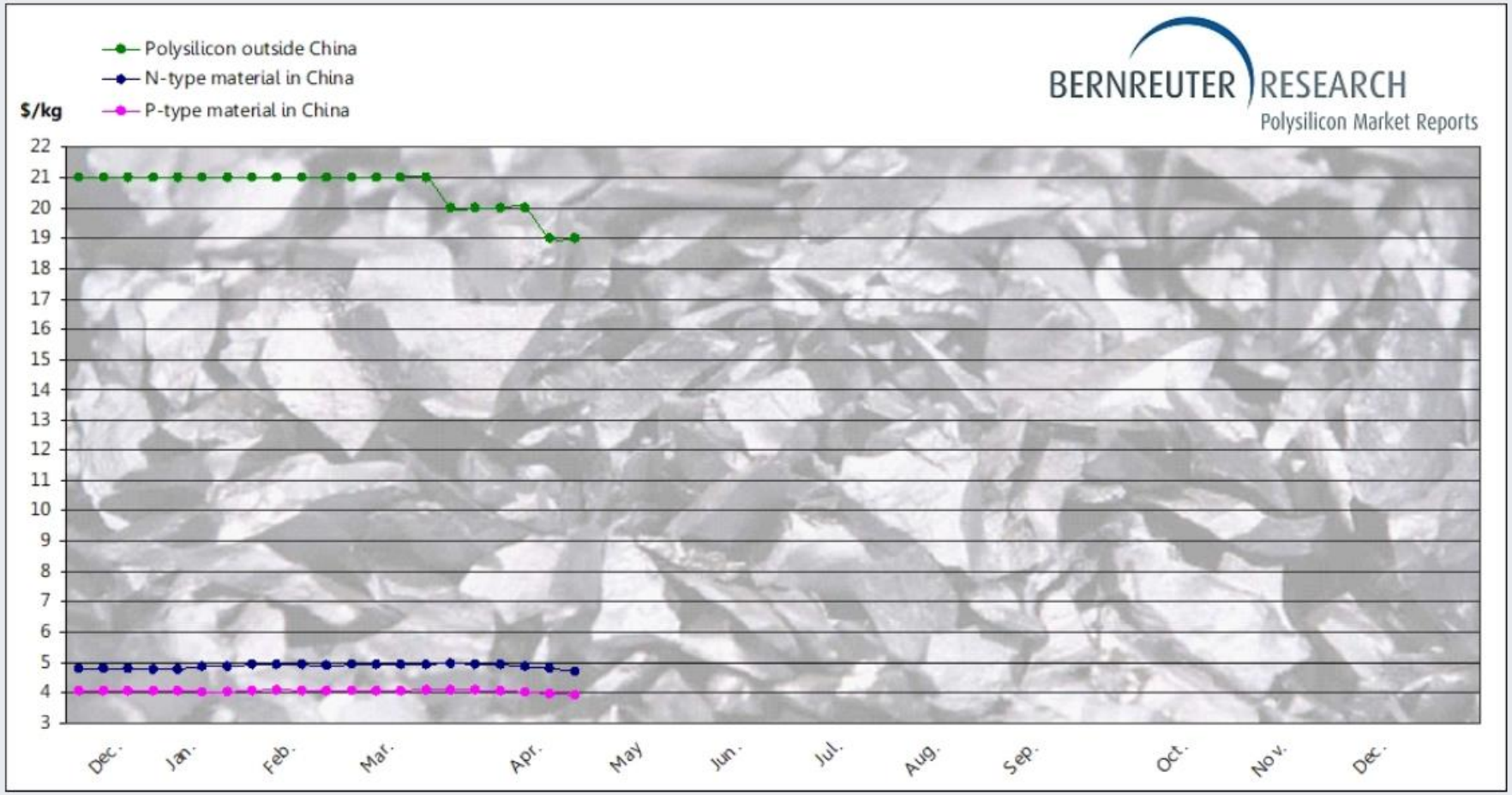
Last update: April 23, 2025



Polysilicon spot prices since December 2024 – Sources: various data providers; Image: Activ Solar; Chart: Bernreuter Research

Chine polysilicon price at 5 $/kg in 2025

Outside at 19 $

Module and shipping costs: impact of poly-Si

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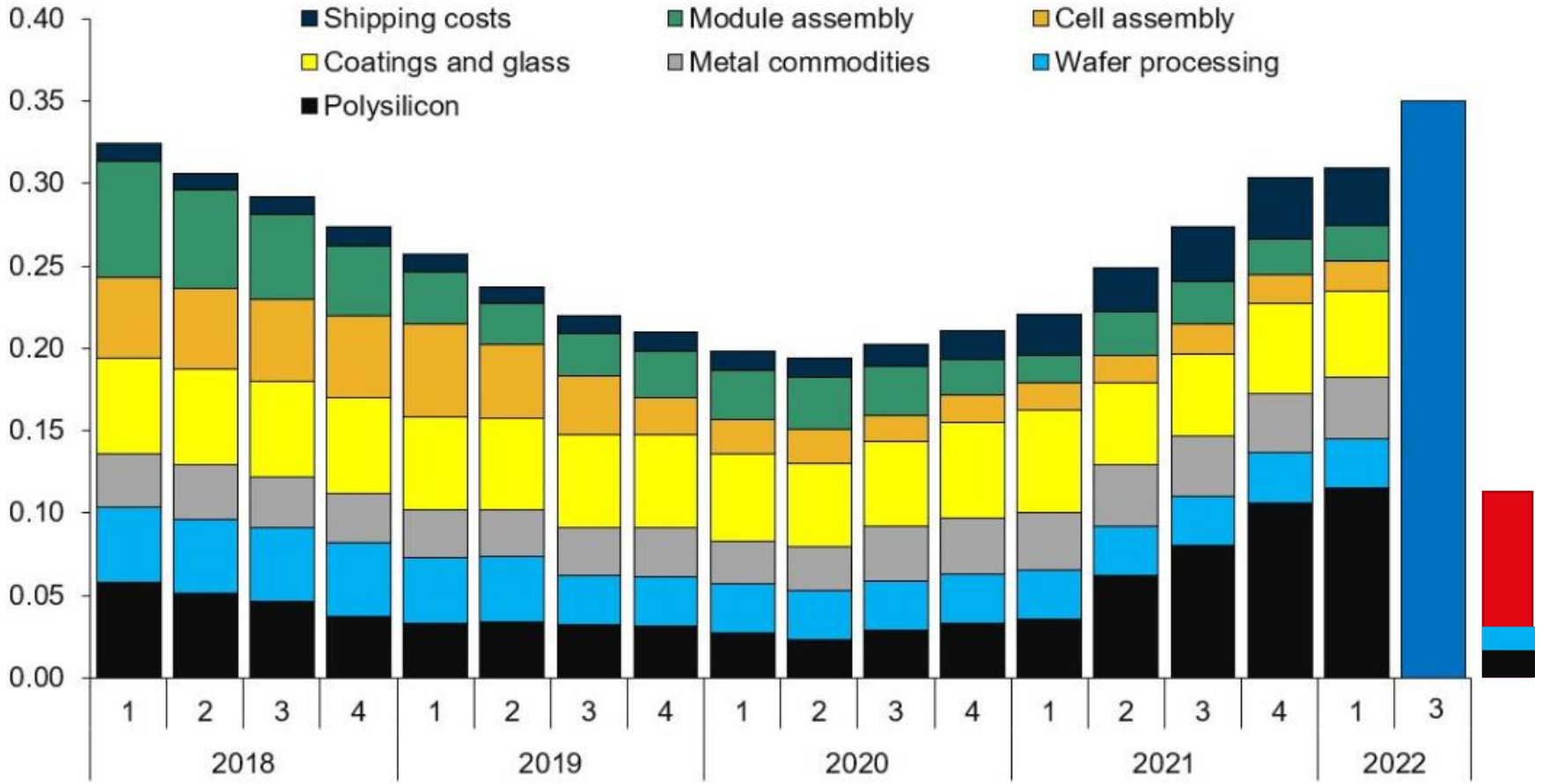
Figure 3: Evolution in solar PV module costs by quarter, 2018-2022*
USD per watt peak (Wp)



*Forecast third-quarter values shown for 2022
Source: Rystad Energy SolarSupplierCube

Production costs (2017)	**2025**
37cts$/W	**10 cts/W**
• 8.7 cts for polysilicon	1.5
• 5.8 cts for wafer	1.5
• 8.6 cts for cells	2
• 13.8 cts for module	5

Costs of Polysilicon (and shipping costs) key in today's module costs

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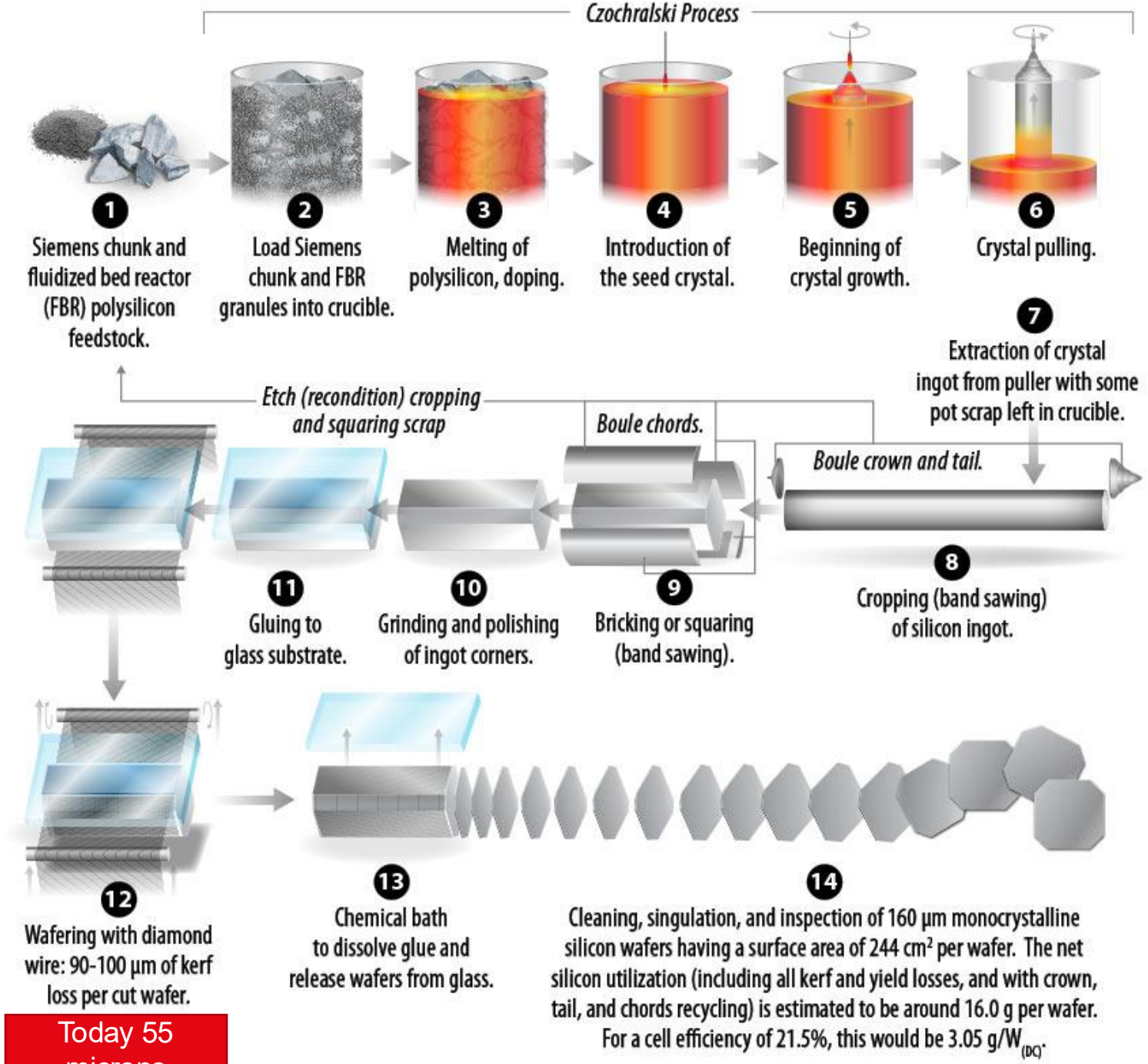
5. From polysilicon to wafers

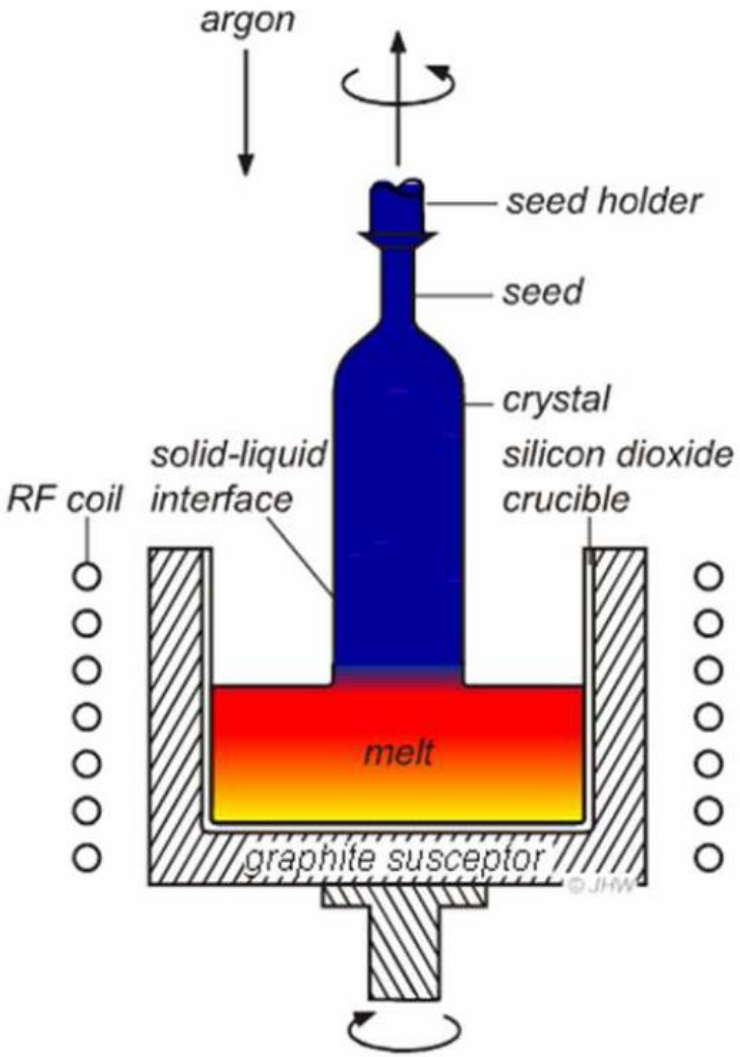


Source NREL

Today 55 microns

5. Ingot fabrication

Monocrystalline silicon



Main process: Czochralski growth.

Polysilicon chunks are melted in a quartz crucible. A small seed crystal with proper crystalline orientation is dipped and rotated in the melt, and then pulled out ! The molten phases crystallises epitaxially with the seed ("liquid expitaxy")

The Si melts by inductively heating with a radio frequency (RF) coil and is kept in a quartz crucible. At the melting point of Si (1415°C), the quartz crucible is soft and is thus held by a graphite susceptor.

Doping is achieved by adding boron or gallium (p-type) or phosphorus (n-type) to the melt.

Typical PV ingots:

- up to 30.6 cm diameter (G12), > 2 meters (or more), > *500 kg* (Increasing every year)
- Control of pulling speed, rotation, heating-cooling, crucible, all essential
-

5. Ingot fabrication: Czochralski process

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Monocrystalline silicon

Quartz crucible and susceptor give rise to oxygen and carbon impurities within the Si liquid and thus also within the Si crystal → High concentration of in Si crystal due to (solid) solubilities around $5x10^{17}$ cm^{-3} (O) and $1x10^{16}$ cm^{-3} (C)

• Crucible can be use multiple times, but metal impurities in the melt tend to increase (so the crucible if change after 3 to 5 times)

- Good initial lifetime, but B-O complex is active for p-type material and needs to be "deactived by special treatment in cell processing.
- Ga doping took the lead for p-type (with more inhomogeneity of dopant)
- N-type ingot grown with P, and now Sb (antimony) as dopant (new trend with Sb, better homogeneity)

In good p-type and n-type wafers lifetime can reach over 1 ms or more for 2-3 Ohm cm material ! Still many kind of defects linked to Oxygen, Carbon, dopants can exist …..

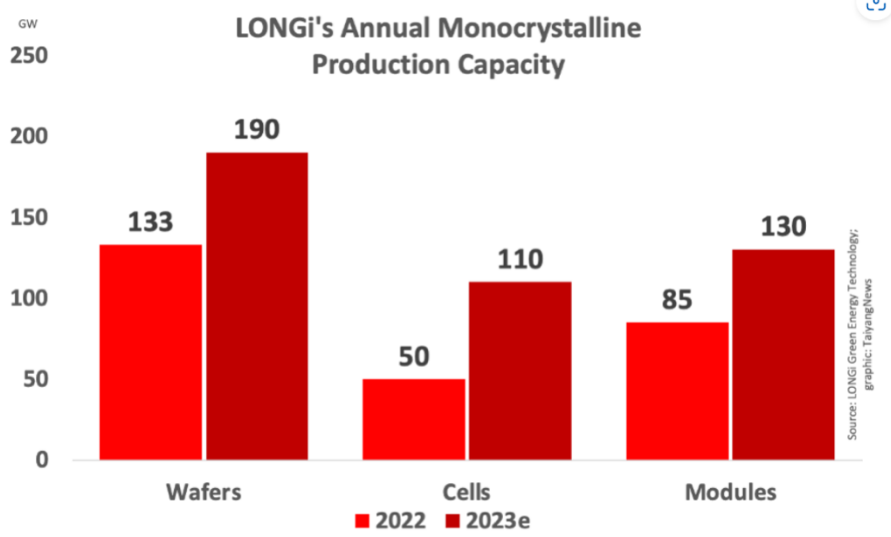
5. Ingot fabrication

2. Ingot

Because of Market shift → almost exclusively mono c-Si ingots

Leader: **Longi,** one of the most valued company in PV

Started with real mass production of c-Si mono
With ~ 65 GW in 2021
~ 130 GW in 2022, 200 GW in 2024



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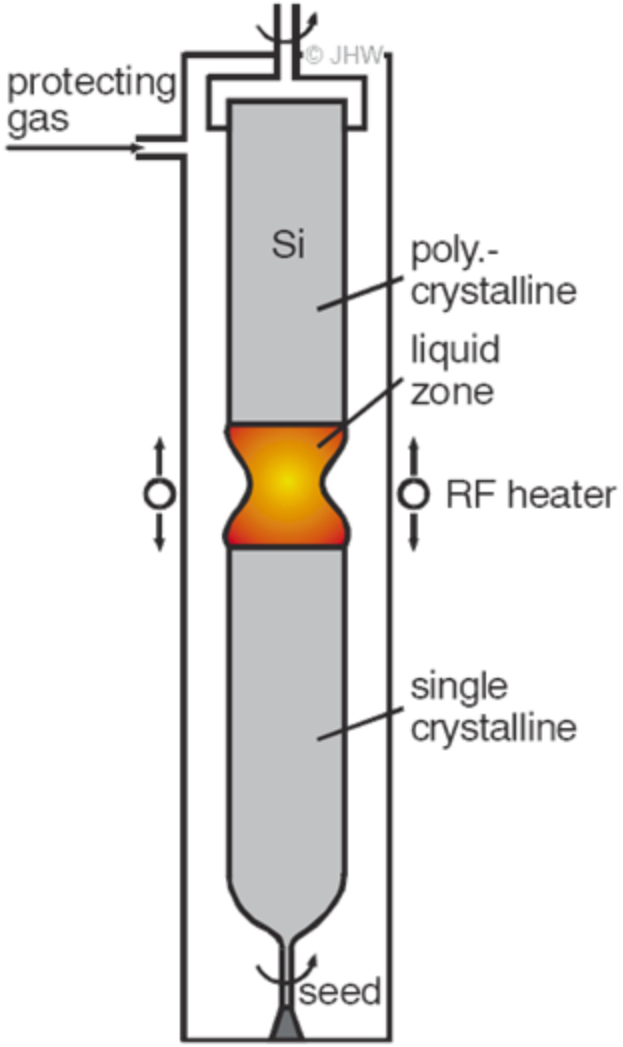
5. Ingot fabrication

Monocrystalline silicon



Float zone [FZ]:

A small crystal seed is melted on the polysilicon rod.
By continuous RF melting and crystallization a single crystal is formed.

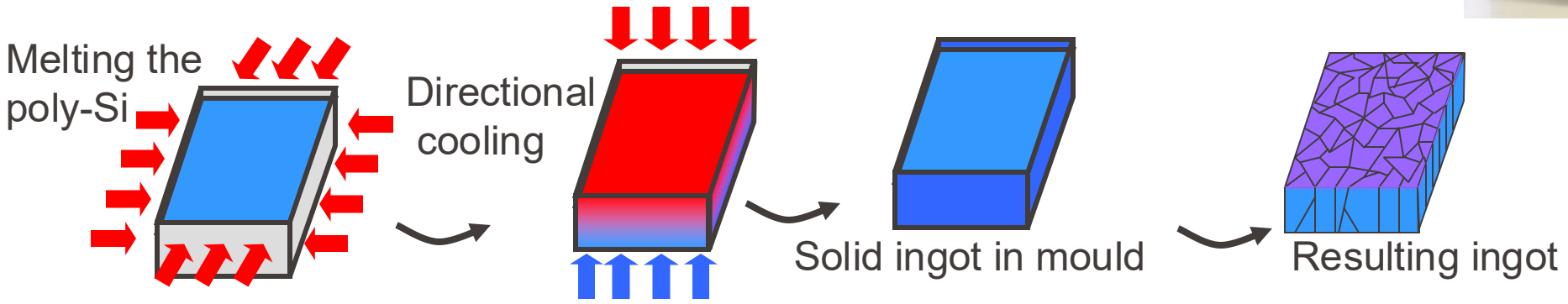
- No impurities through contact with crucible
- Crystal fixation only at one end

Higher cost. High lifetime wafers,
ideal for testing purpose! Not used in production for PV
(but for some electronic applications)

The float zone process is capable of producing silicon with 100 times greater resistivity and 10,000 times greater purity than the commonly-used Czochralski growth process. Float zoning involves repeated refining of a polycrystalline rod, resulting in an increasingly pure material. The purification process relies on the higher solubility of impurities within the liquid Si than in the solid Si (i.e. on a low segregation coefficient around 10-4 to 10-5).

5. Ingot fabrication

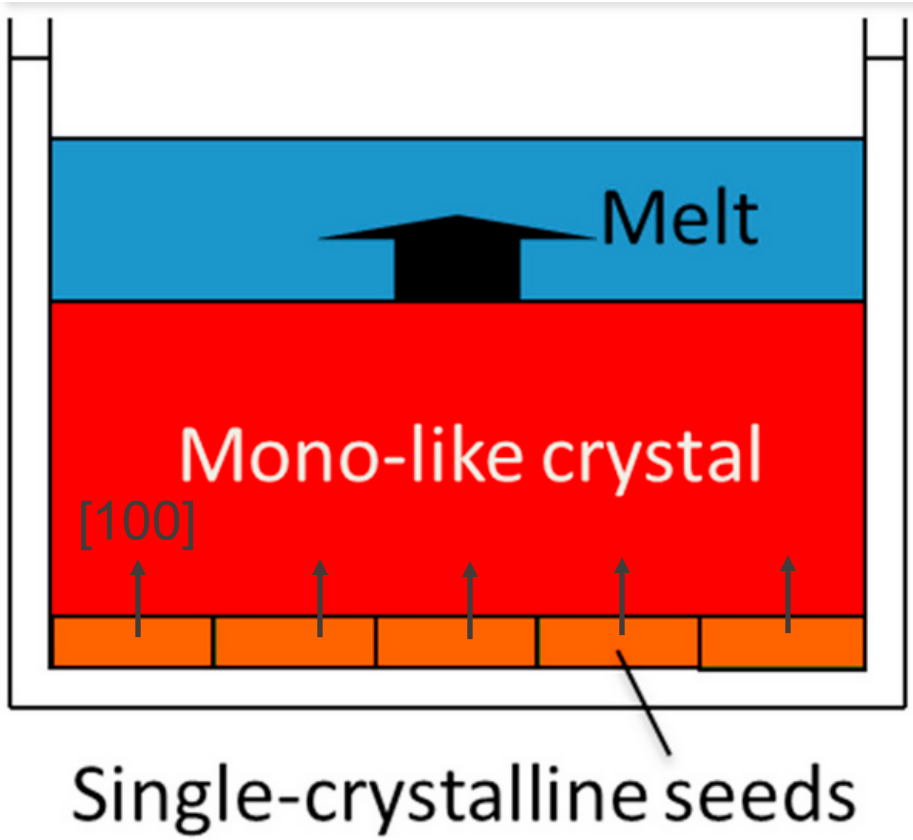
Solidification process for multicrystalline silicon



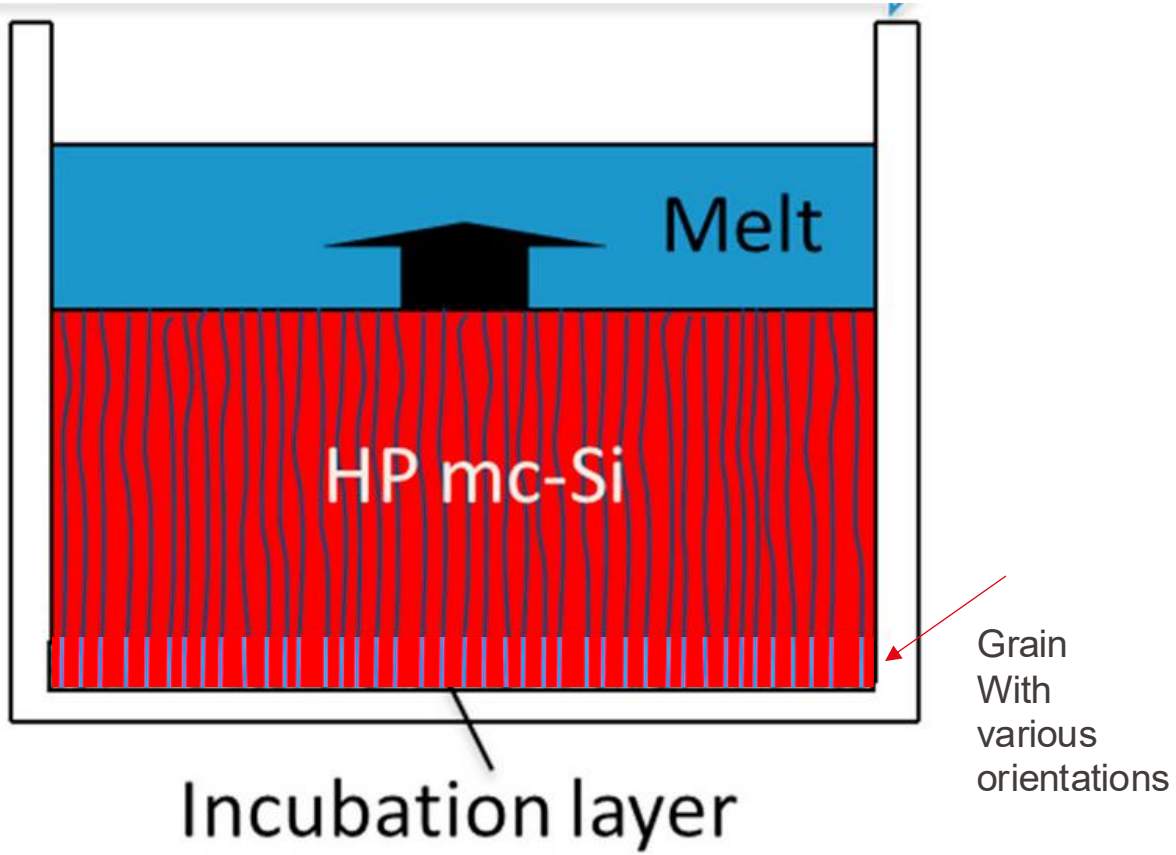
5. Ingot fabrication

Multicrystalline silicon

Improvement of quality: use a «seed» crystal which defines orientation by liquid epitaxy growth from the molten silicon



Mono-like



High performance multi

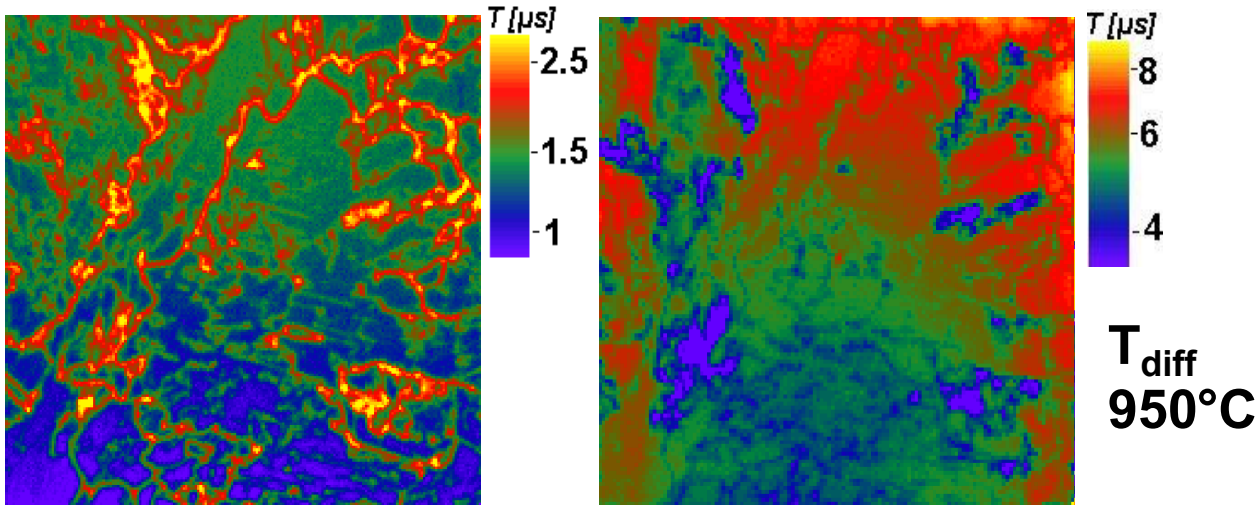
5. Ingot fabrication

Gettering

Reminder: in multi-Si the lifetime is not homogenous!

Bottom part of multi-Si ingot

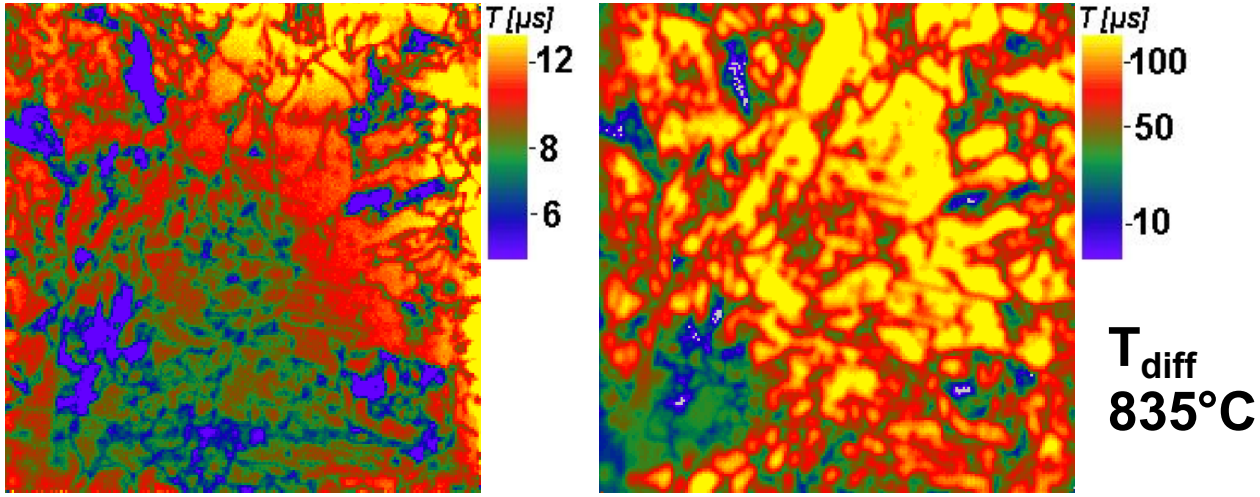
Initial



T_{diff} 950°C

Lifetime is measured using PLI (PLI = 1500 x 10^{12}/cm^2 1 Sun)

T_{diff} 900°C

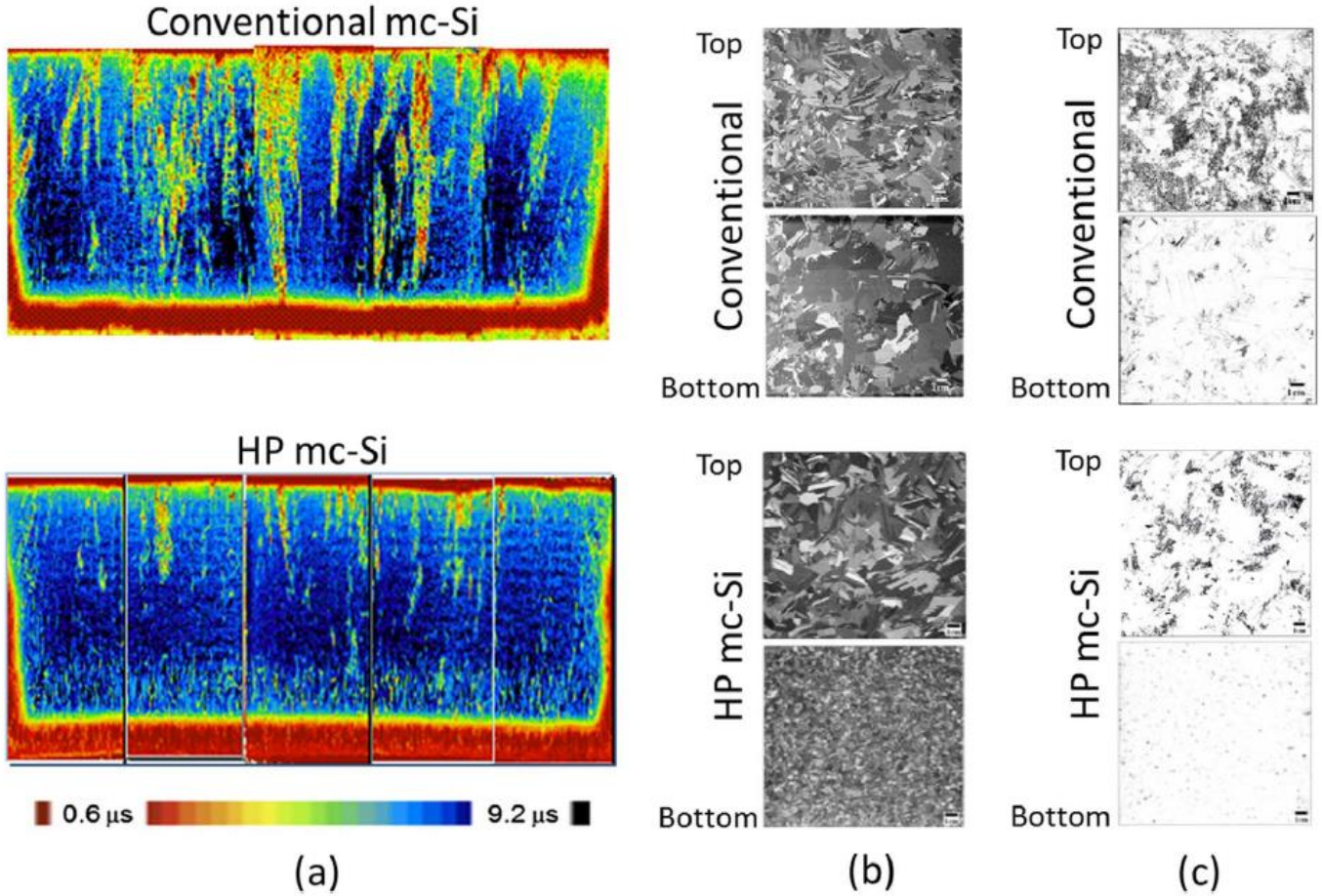


T_{diff} 835°C

5. Ingot fabrication

High performance (HP) mc-Si

Same as quasi mono, but with a seed multi-crystalline wafer, which allows smaller grain size → suppression of «dangerous dislocations»

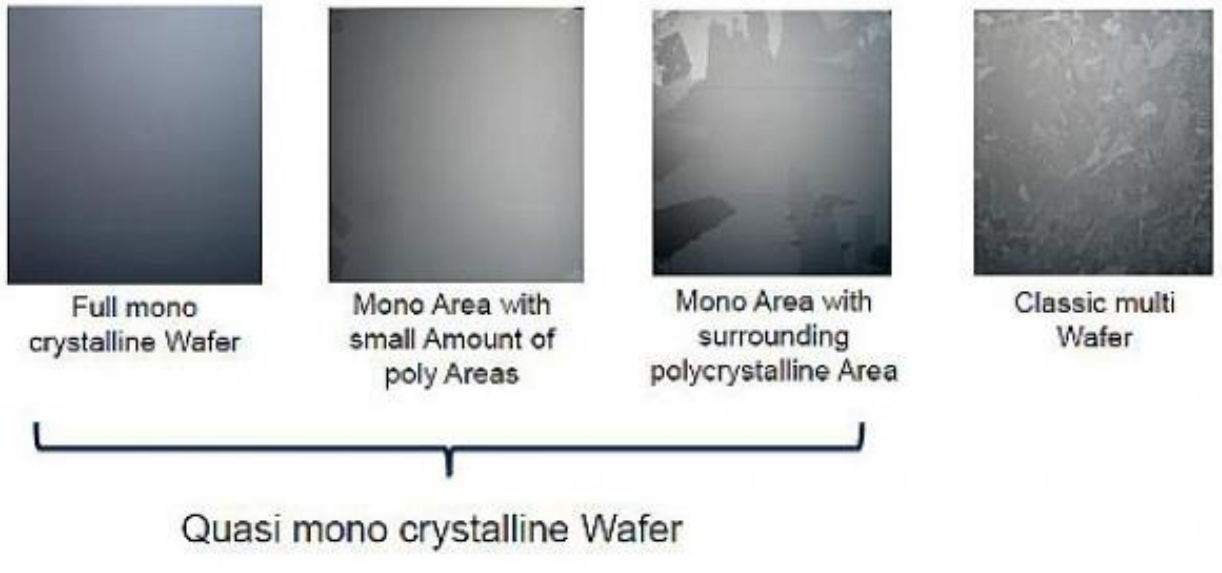


C.W. Lana et al., Journal of Crystal Growth 2016

5. Ingot fabrication

2. Ingot

Quasi-mono wafers



Recrystallisation process with monocrystalline wafers as seed!
Large part of the ingot can be mono-crystalline → ***Quasi-mono c-Si***

++ Wafers with (100) orientation can be etched with "random pyramids"
++ high current and reasonable lifetime

-- high density of dislocations, part of the ingot can be multi-crystalline (lifetime depends on process)

5. Ingot fabrication

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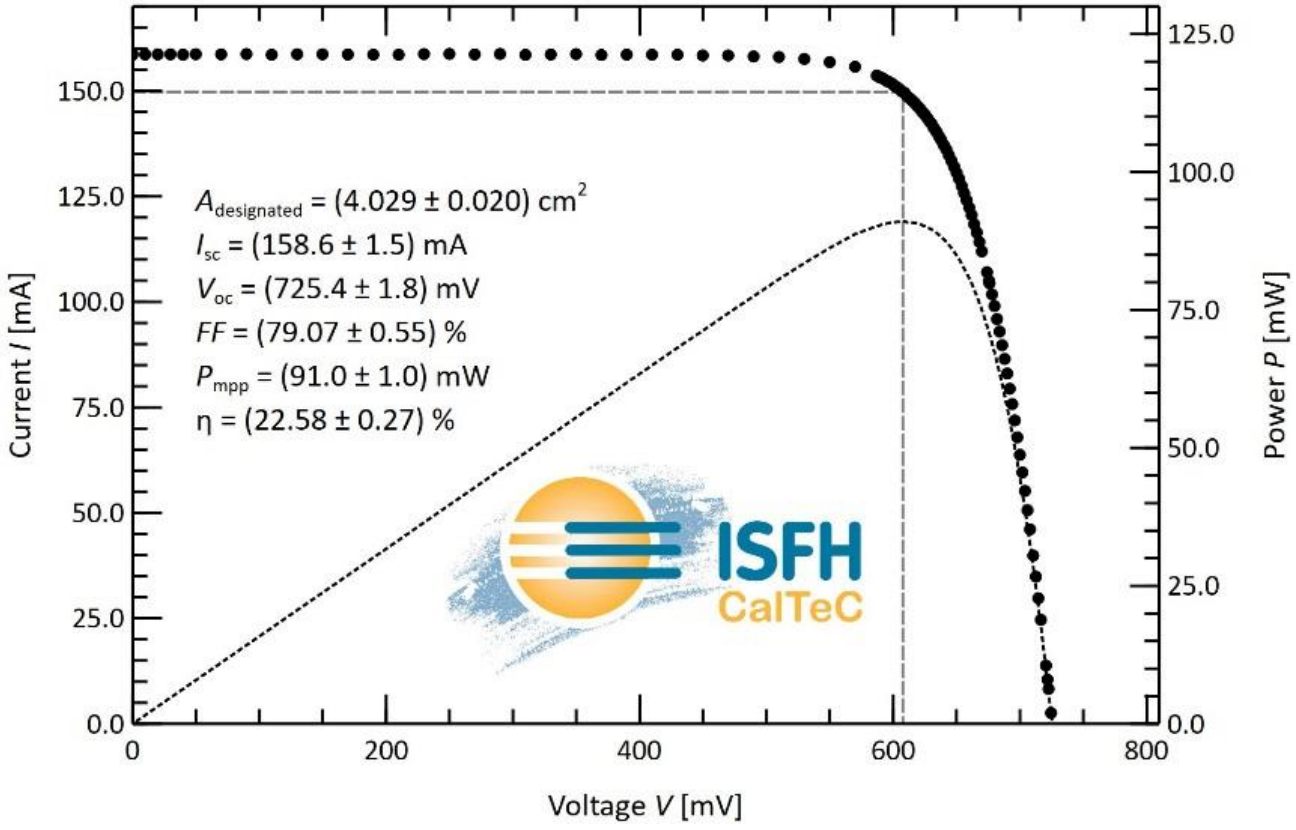
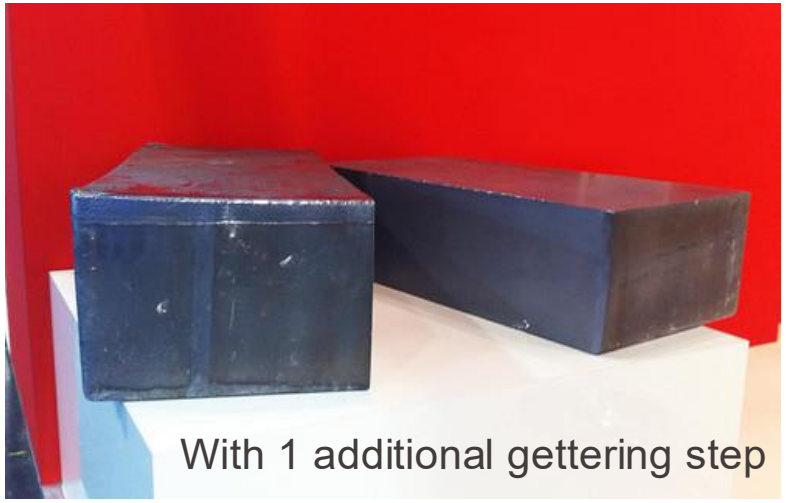
World record Quasi-Mono cell at 22.6% (2019)

Usage of gettering and of high-efficiency heterojunction process




With 1 additional gettering step

22.6% certified record for cast Quasi-Mono, 4 cm2 cell!

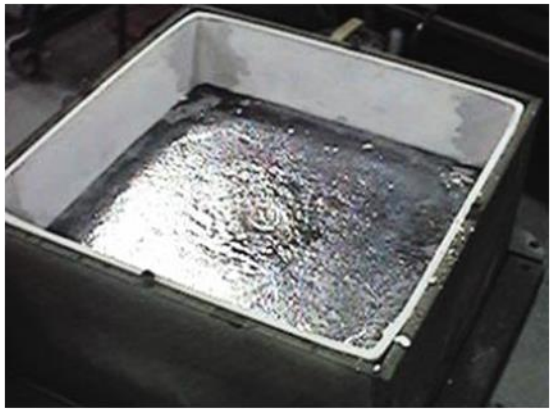
J. Hascke et al. IEEE WCPEC-7

QEERI
معهد قطر لبحوث البيئة والطاقة
Qatar Environment & Energy Research Institute
جامعة حمد بن خليفة
HAMAD BIN KHALIFA UNIVERSITY

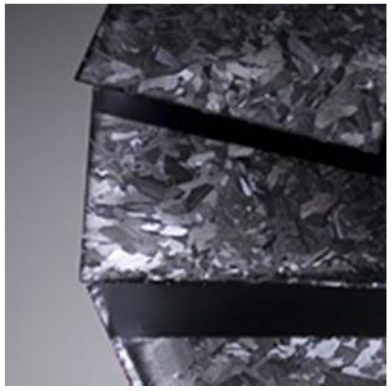
6. Wafering

Wafer production step

Poly-Si → Ingot solidification → Bricketing →



→ Gluing → Wafering → Cleaning

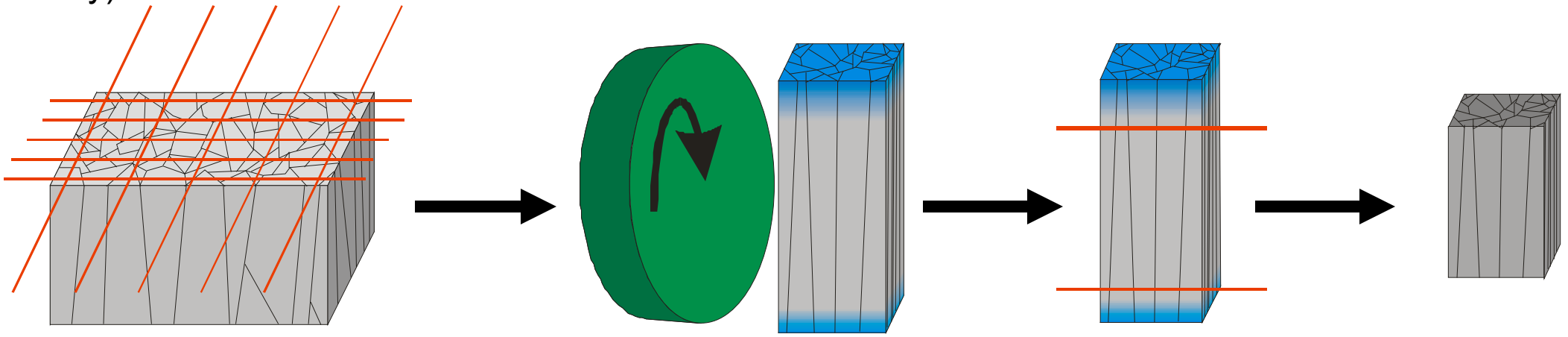


6. Wafering: first needs to make bricks «bricketing, polishing and cropping»

2. Ingot

- For round mono Si ingots, the top and bottom part are cropped. The ingot is «squared»
- For mc-Si large's block
  - The ingot's edges have to be removed (diffusion of contaminants from crucible)
  - Top and bottom of each brick is cropped (bottom: diffusion from crucible, top: too high level of dopants and impurities due to segregation)
- The sides and edges of each brick are ground (removal of cracks induced during bricketing to increase later the wafer strength, and to have a better control of the bricks dimensions)

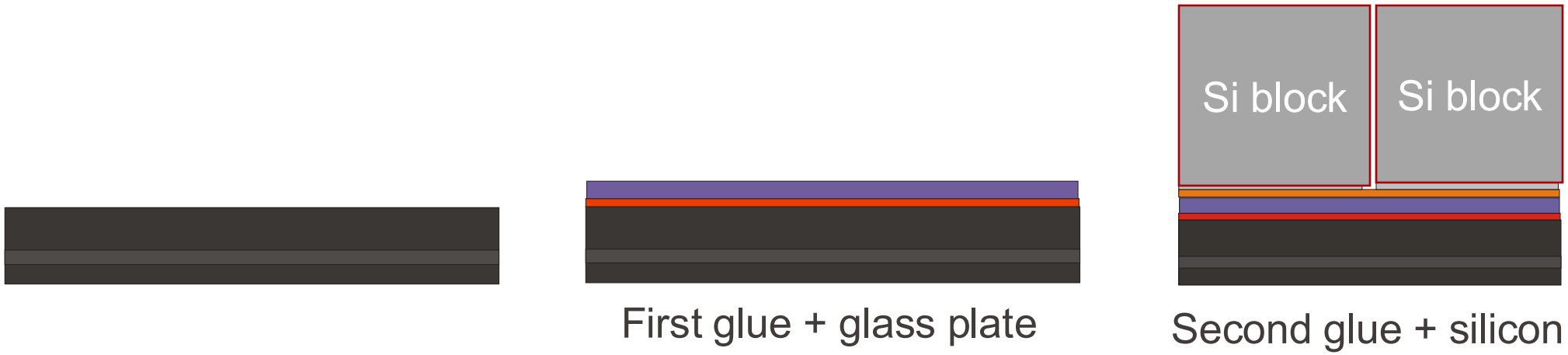
- The parts that have been sawn away are usually molten again
- The aim is to keep the highest amount of material, while being sure that the silicon has a high quality
- Type of saw used: band saw (fast and easy, large kerf loss) or wire saw (slower, less kerf loss, needs slurry)



6. Wafering

Gluing

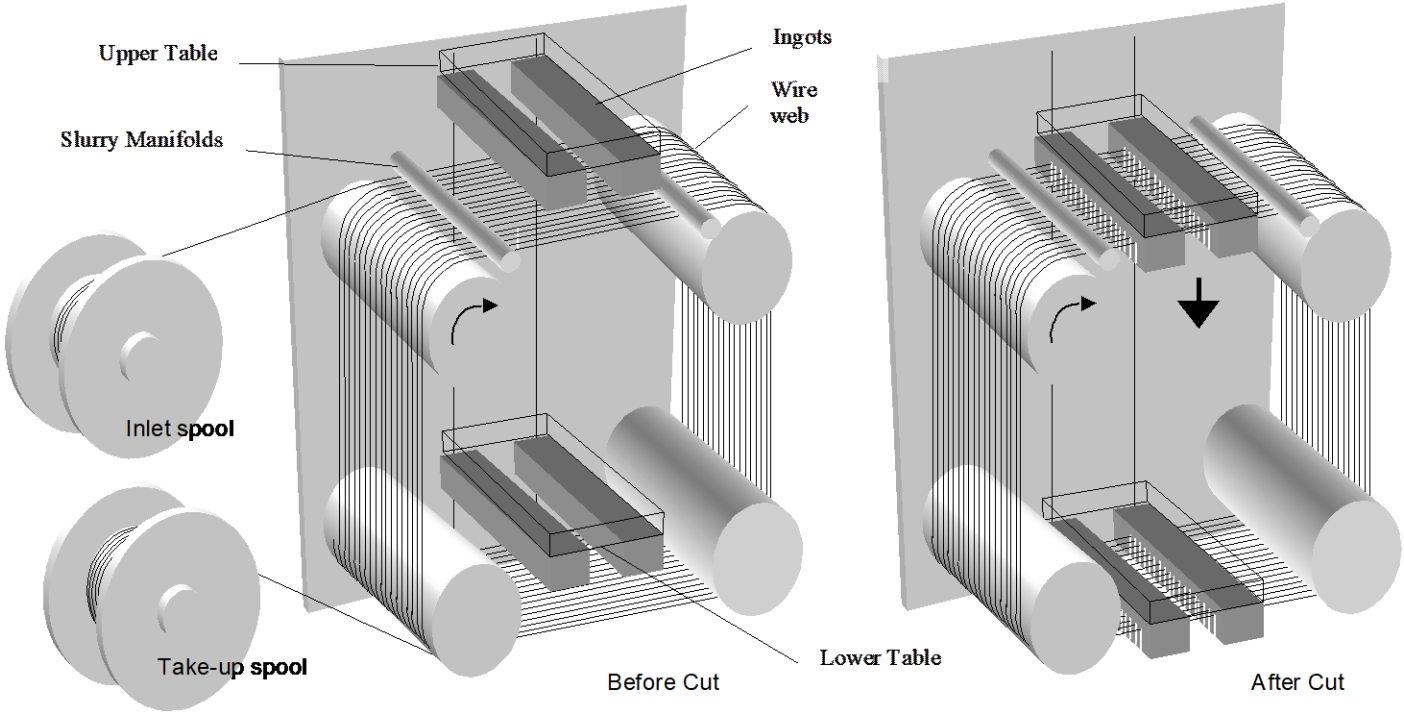
- Aim: fix the silicon brick to the saw holder
- Used glue: epoxy. Hot water (+ additives) is used to detach the wafers (epoxy interface becomes weak)



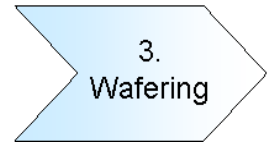
6. Wafering

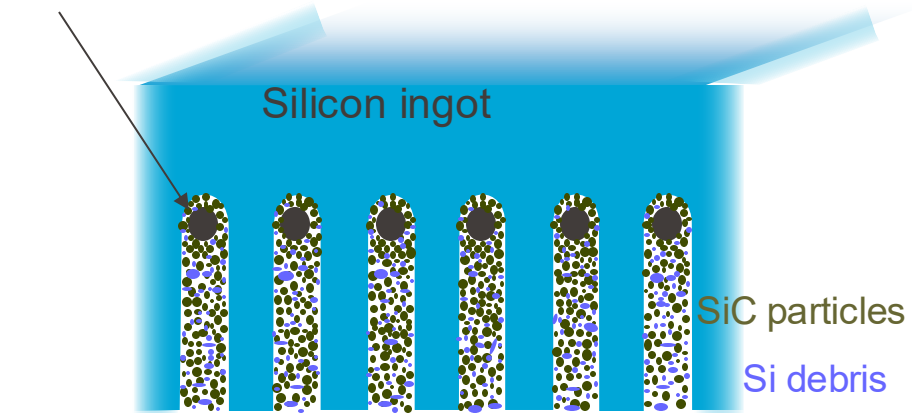
Prof. Christophe Ballif

All wafers are sawn today with multi-wire sawing (MWS).
Meyer-Burger in Steffisburg (BE) (now PSS) and Applied Materials (VD) were world leaders for such equipment (before beeing heavily copied)

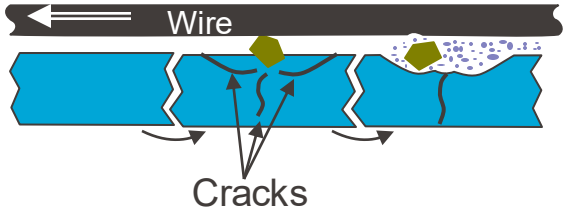


6. Wafering by multiwire sawing





Scratching, indentation, and cracking induced by wire pressure on SiC particles



Standard sawing with SiC particles (until 2017)

- Slurry: mixture of lubricant (PEG) and abrasive SiC (d_{50}: 7 – 10 µm)
- Steel wire (Ø 100 – 140 µm), running at 10-15 m/s
- Time needed to complete a cut : 7 – 10 hours
- Length of silicon ingots that can be sawn in one cut: 1 – 2 meters (4x50 cm)
- Amount of slurry needed: 300-600 litres per run
- Almost 50 % of the silicon is lost during this step

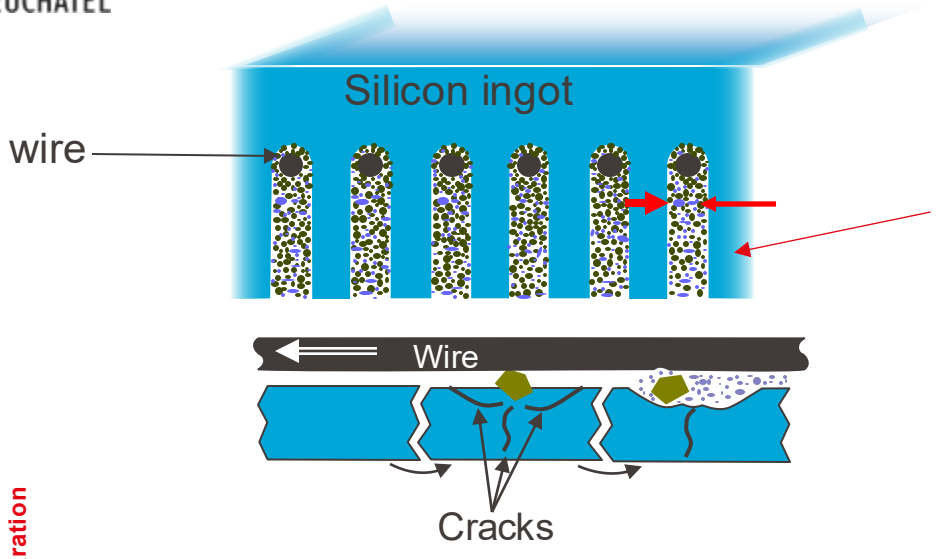
Possible problems:
- wafer falling
- off-spec wafers
- wire breaking

Challenge: saw thinner wafers with less kerf loss

If the sawn wafers are too fragile, they break down during the cell production

6. Wafering with SiC slurry

Prof. Christophe Ballif



- Kerf loss ~ wire diameter + 2 times SiC particles ~130-180 µm

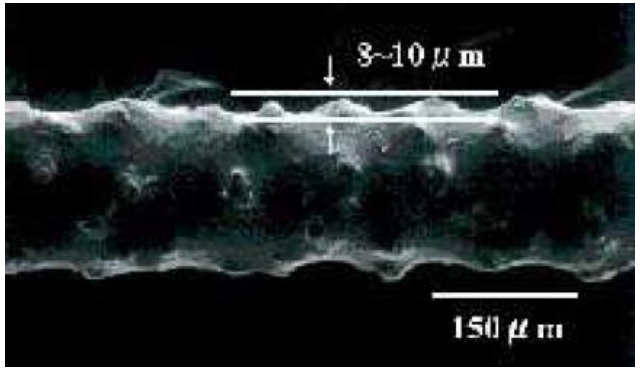
For a typical industrial saw in 2015, a wafer thickness of 190 µm and kerf loss of 150 µm translates into 5500 wafers cuts in a typical production too with an annual capacity of ~ 13-15 MW.

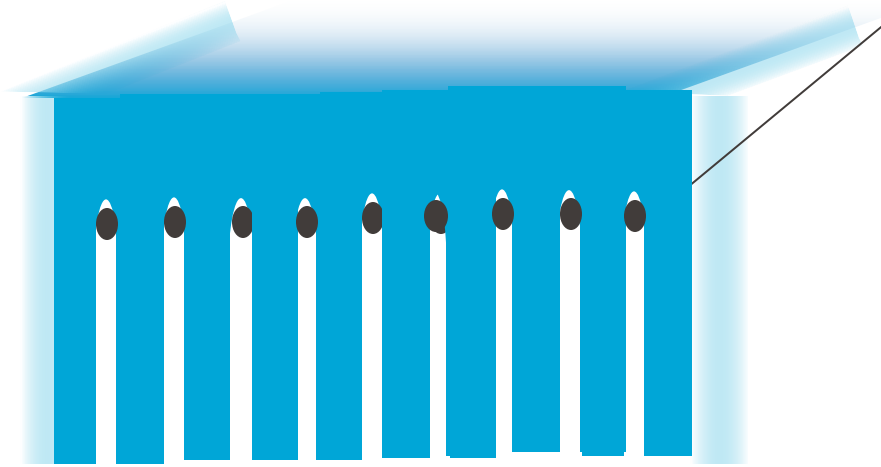
6. Wafering

The revolution of diamond wire sawing

Diamond sawing: Diamond-plated wire: diamond particles are bound to the wire

- The sawing is much faster (2-3 times faster)
- The wire can be used several times
- Much less total thickness variation
- The slurry is replaced by a lubricant
- But the wire is more expensive





- Today, diamond wire kerf losses for mono down to 50 microns (wires today at 37 microns !!) against 130-180 for slurry based sawing. Wafers from 110 to 150 micron thick

→ 70-100 % more wafers than 6 years ago !

In two years (2017-2018) most companies have shifted to diamond wire sawing.

Important

- In 2025, typical wafer thickness

150 microns PERC

130 microns TOPCON

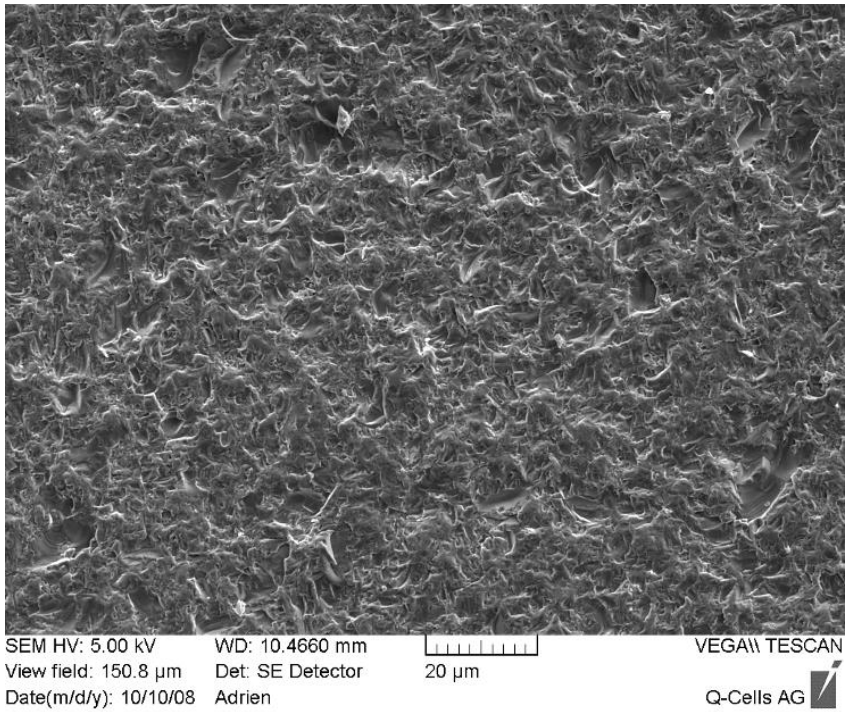
110 microns Heterojunction

The better the passivation of surfaces, the thinner you can become. But: challenges in automation for thin wafers (breakage) , and if too thin start to loose current because of indirect bandgap of silicon

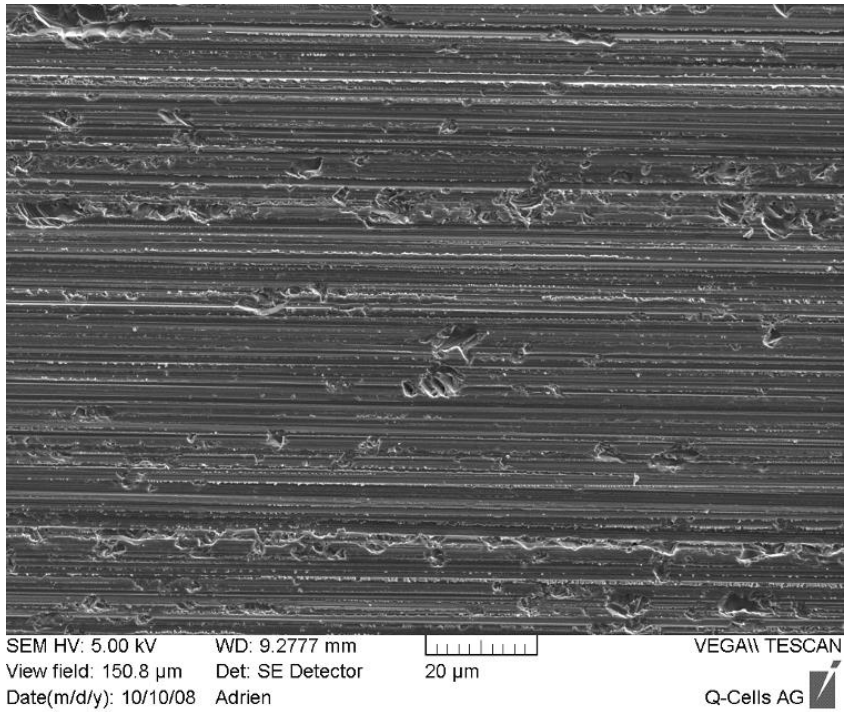
6. Wafering

Prof. Christophe Ballif

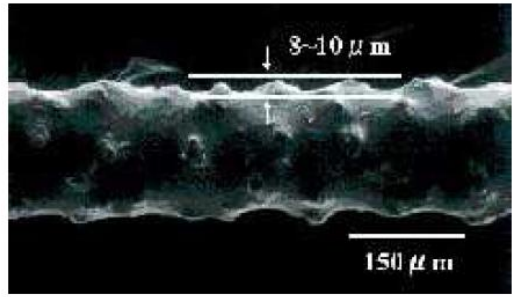
Slurry cutting



Diamond sawing



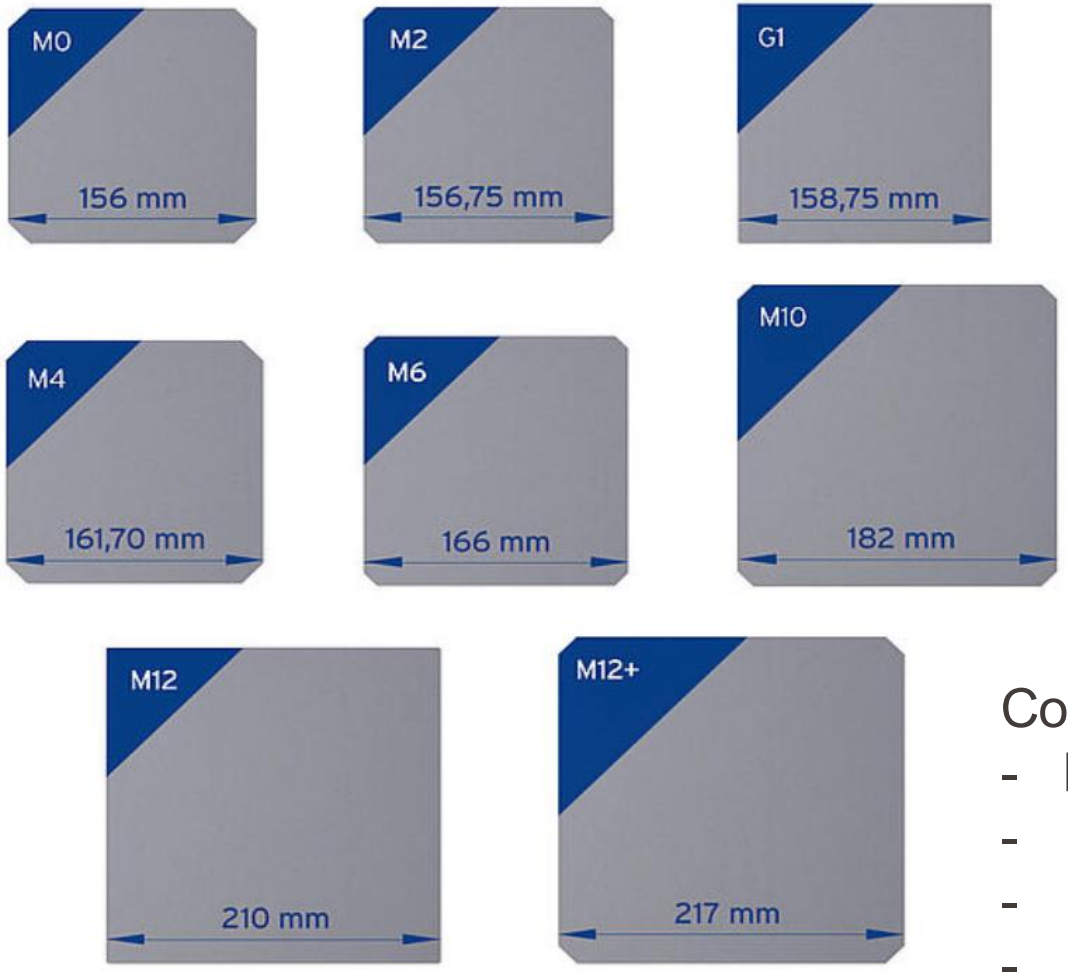
Source:
A. Bidiville
Proc. EU PVSC,
Hamburg 2009

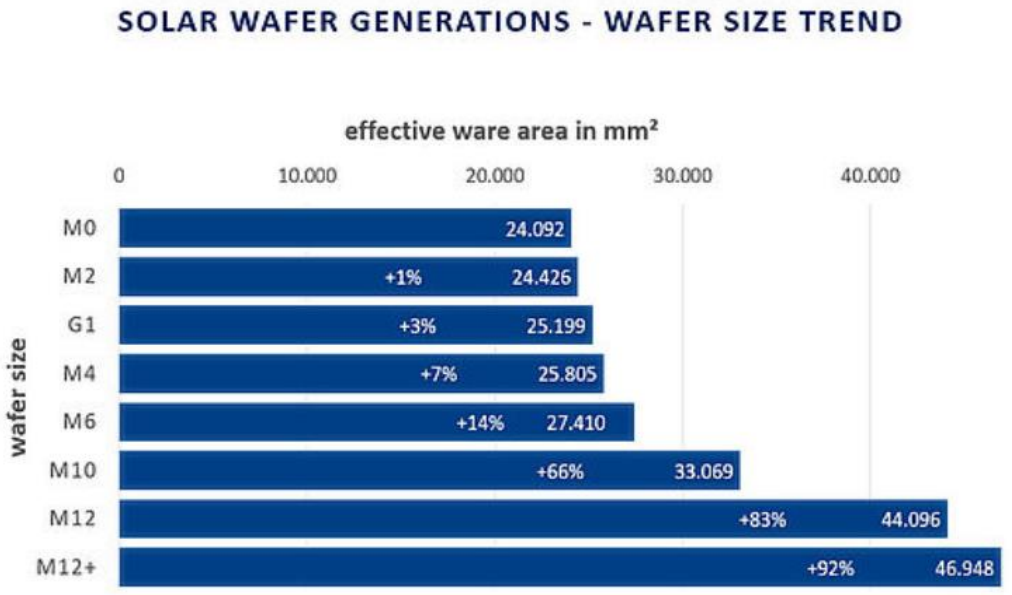


SEM picture of the surface of a) a wafer cut with a standard slurry made of SiC and PEG and b) a wafer cut with a diamond wire. On contrary to the diamond-wire sawn wafer, the surface of the slurry sawn wafer does not show clearly the wire direction during the cut. The surface of the diamond-wire sawn wafer shows grooves which have been plastically deformed, but also parts that have been chipped off.

6. Wafering and crystal growth

The trend in wafer size





Companies are shifting to larger wafers:

- Higher ingot productivity
- Increased productivity of the cell process.
- Less cells edge effects
- Larger modules (less innactive edges of modules)

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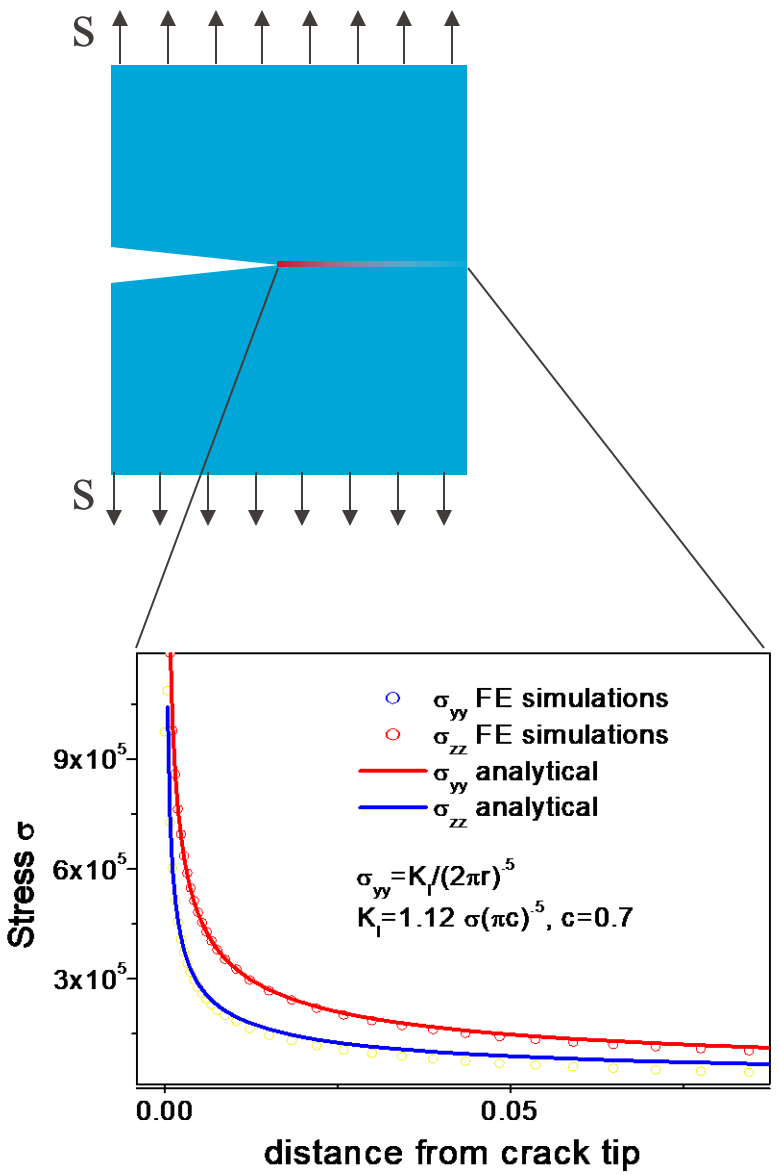
7. Mechanical properties of silicon

Sharp cracks

- Silicon is a hard, brittle material
  - It is hard to machine;
  - It cannot sustain large deformation.
- Cracks make the wafers weak:
  - They act as stress concentrators, the stress at the crack tip is much larger than in the bulk of the sample. It can lead to crack propagation and sample breakage (even at low stress).
  - Fracture mechanics: the critical stress depends on the crack shape and size, the applied load and the material.
- It is impossible to saw wafers without cracks!
  - Thus, to have stronger wafers, the cracks have to be smaller.
  - This is why you need to etch wafers (more or less deeply)



7. Mechanical properties of silicon

If a sharp crack of depth *a* is present in Si, which tensile stress σ_c is needed to start the crack propagation?

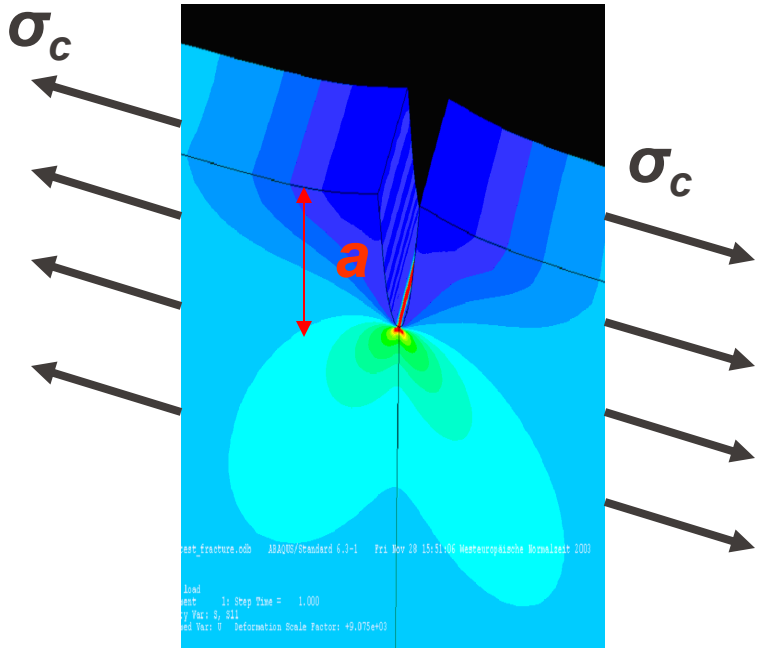
semi-infinite plate

$$\sigma_c = 0.82 (\pi a)^{-1/2} K_{IC}$$

K_{IC} = fracture toughness

For Si, K_I = 0.8-0.9 MPa $m^{1/2}$ along (111) planes
For GaAs, K_I = 0.31-0.46 MPa $m^{1/2}$
along {110} planes (cleavage anisotropy)

Example:
10 micron crack in Si has strength of 140 MPa



Crack opening, mode I

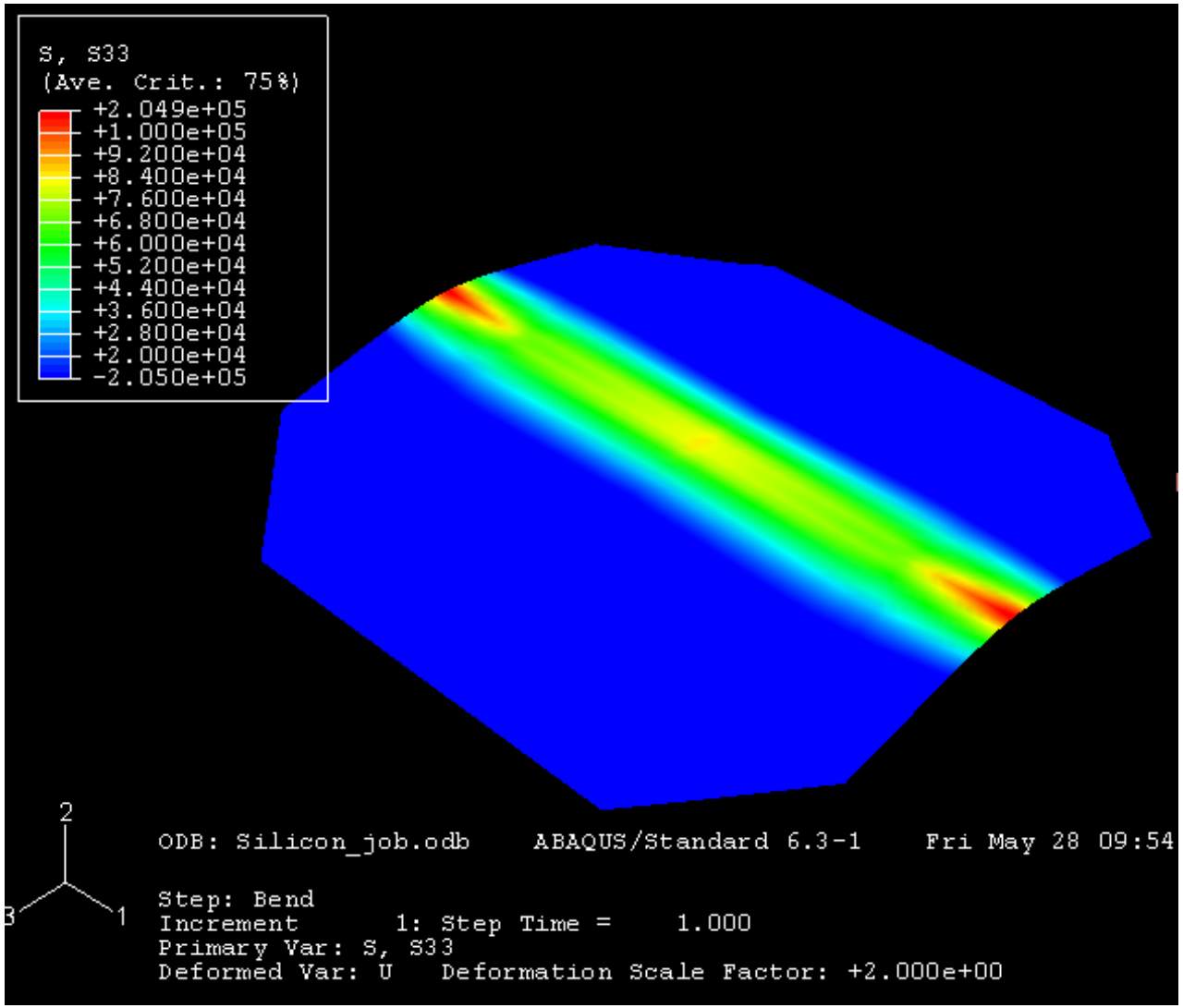
7. Mechanical properties of silicon

An application example

Example of a **200 µm** thick cell stressed with a deformation of 5 mm in the middle

Surface tensile stress up to **200 MPa**

A 5 µm crack will lead to complete wafer breakage



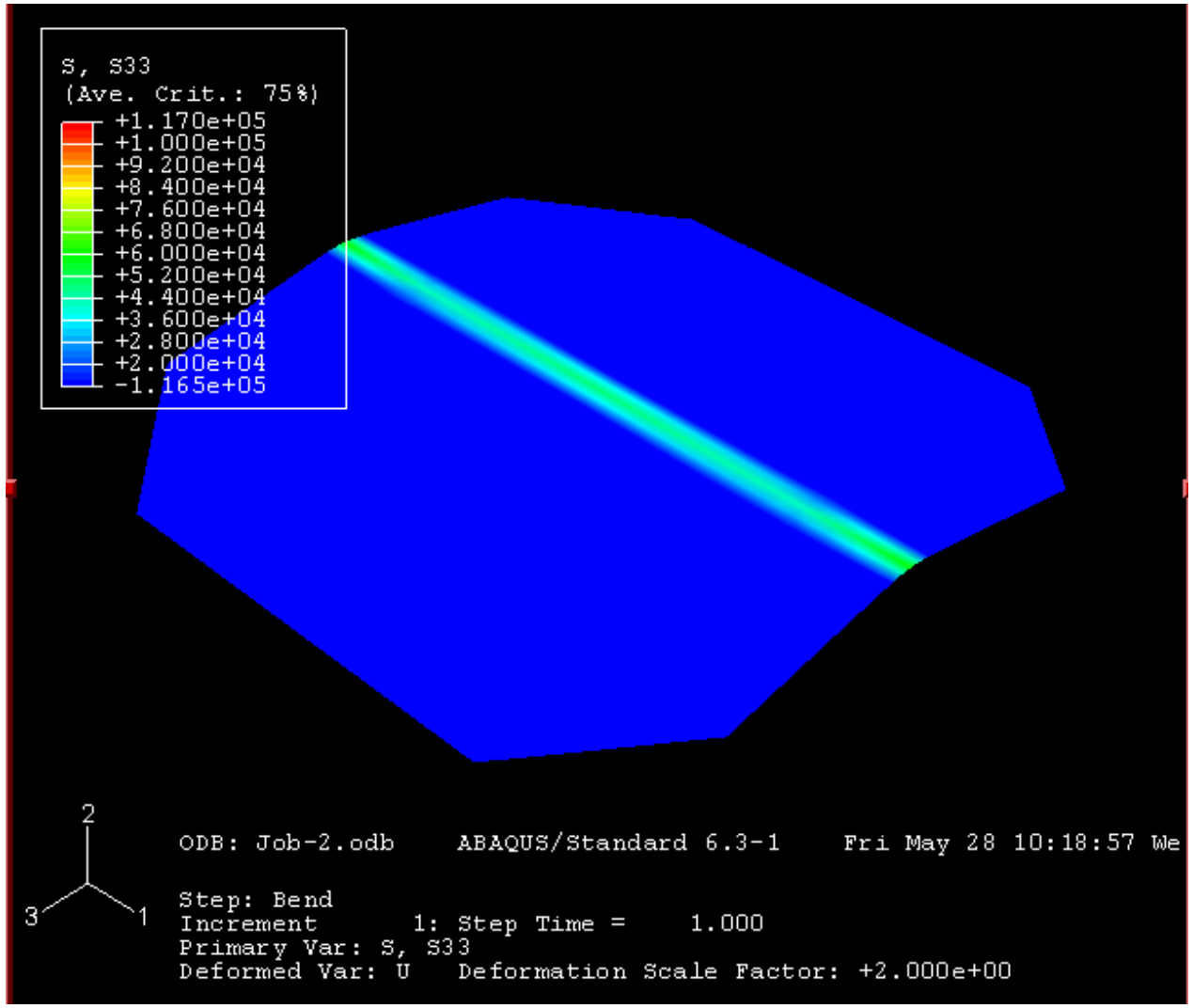
7. Mechanical properties of silicon

The thinner, the better

Example of a **50 µm** thick cell stressed with a deformation of 5 mm in the middle

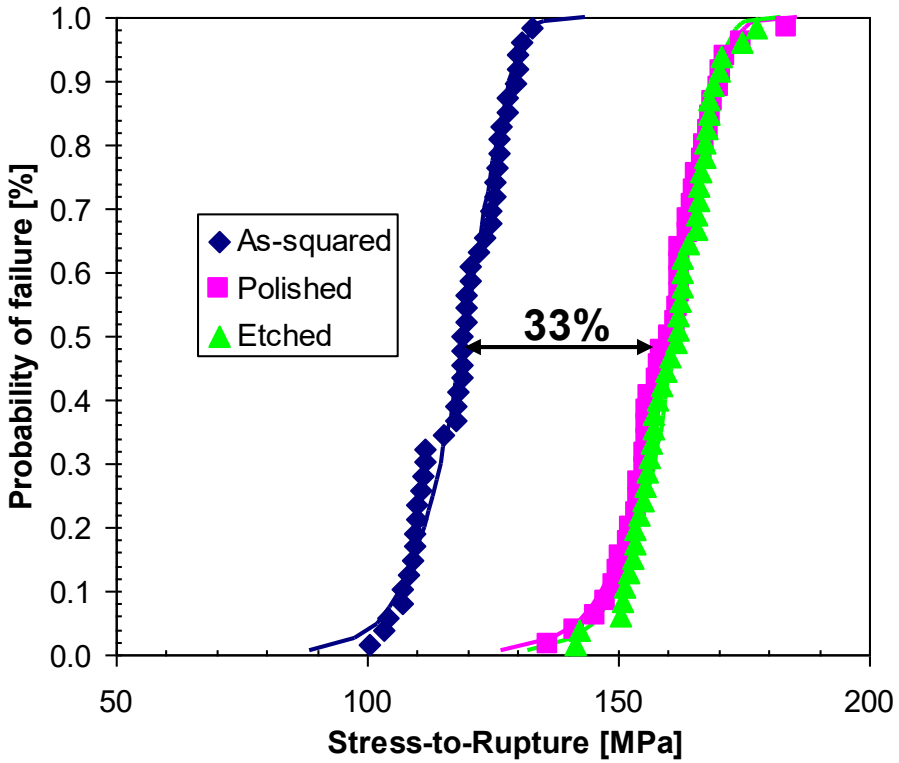
Same scale:
tensile stress up to **100 MPa**

A 20 µm deep crack would lead to wafer damage

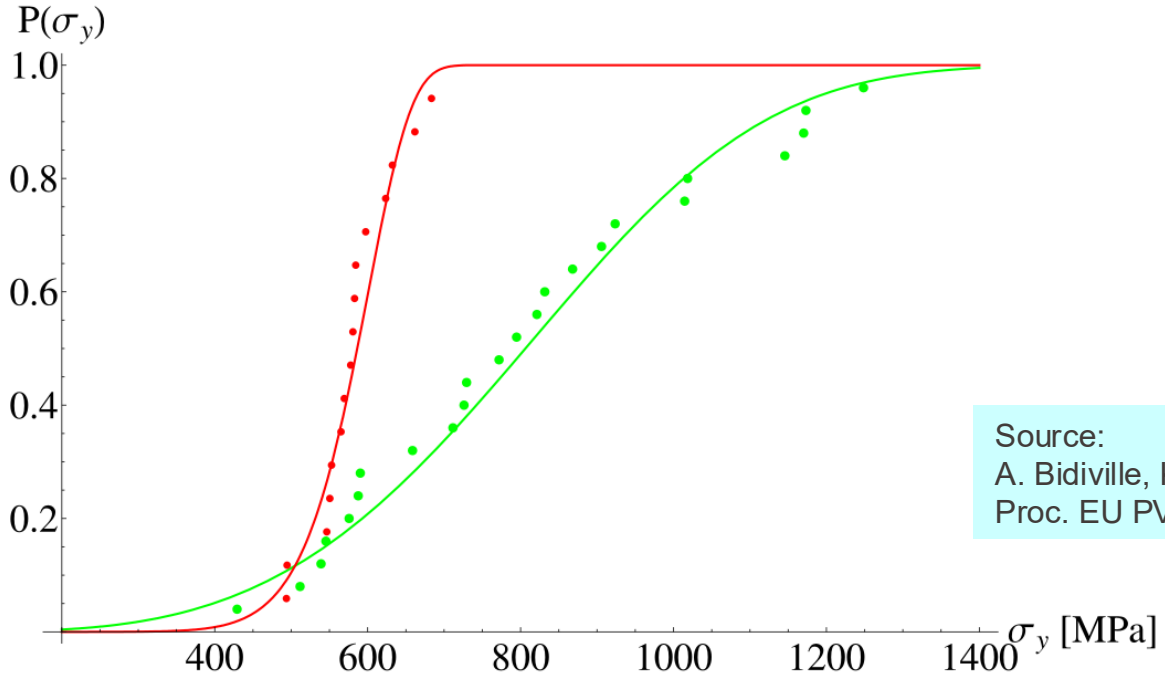


7. Mechanical properties of silicon

Effects of edge improvement on wafer strength



Effects of small (green) and large (red) abrasive

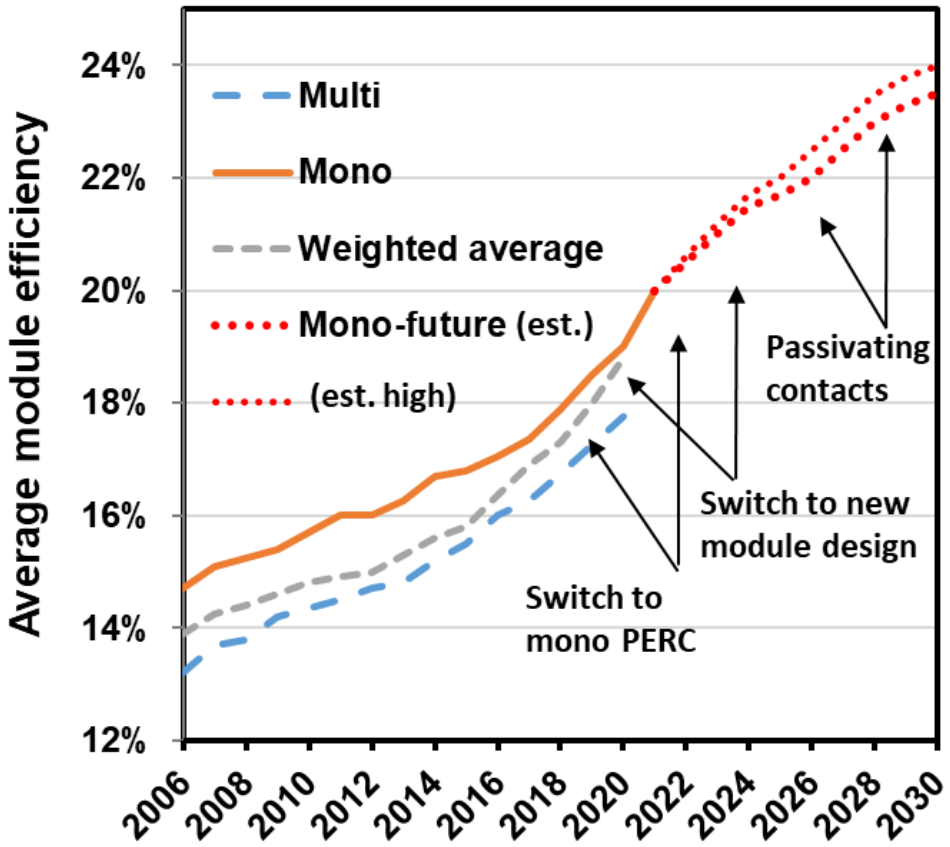


Source:
A. Bidiville, K. Wasmer
Proc. EU PVSC

- Because of sawing induced cracks and possible material defects from the growth Si wafer can break.
- Proper saw damage removal (10-15 microns) is important to avoid electronic defects in the cells and to avoid breakage during processing (most cell and module yield losses)
- Under price pressure industry now succeeds with 110-130 microns in thickness wafers .
- Once encapsulated, solar cells are much less subject to breakage!

8. A reminder on Grey energy

Less silicon usage



Data source: HIS Market 2019, Fraunhofer report and Ballif et al. Nature Review materials 2022

0.3- 0.4% annual module absolute efficiency improvement

Gain in module efficiency

- much less silicon usage per W
- Reduced system costs
- More money for management or transformation (power-to-x)

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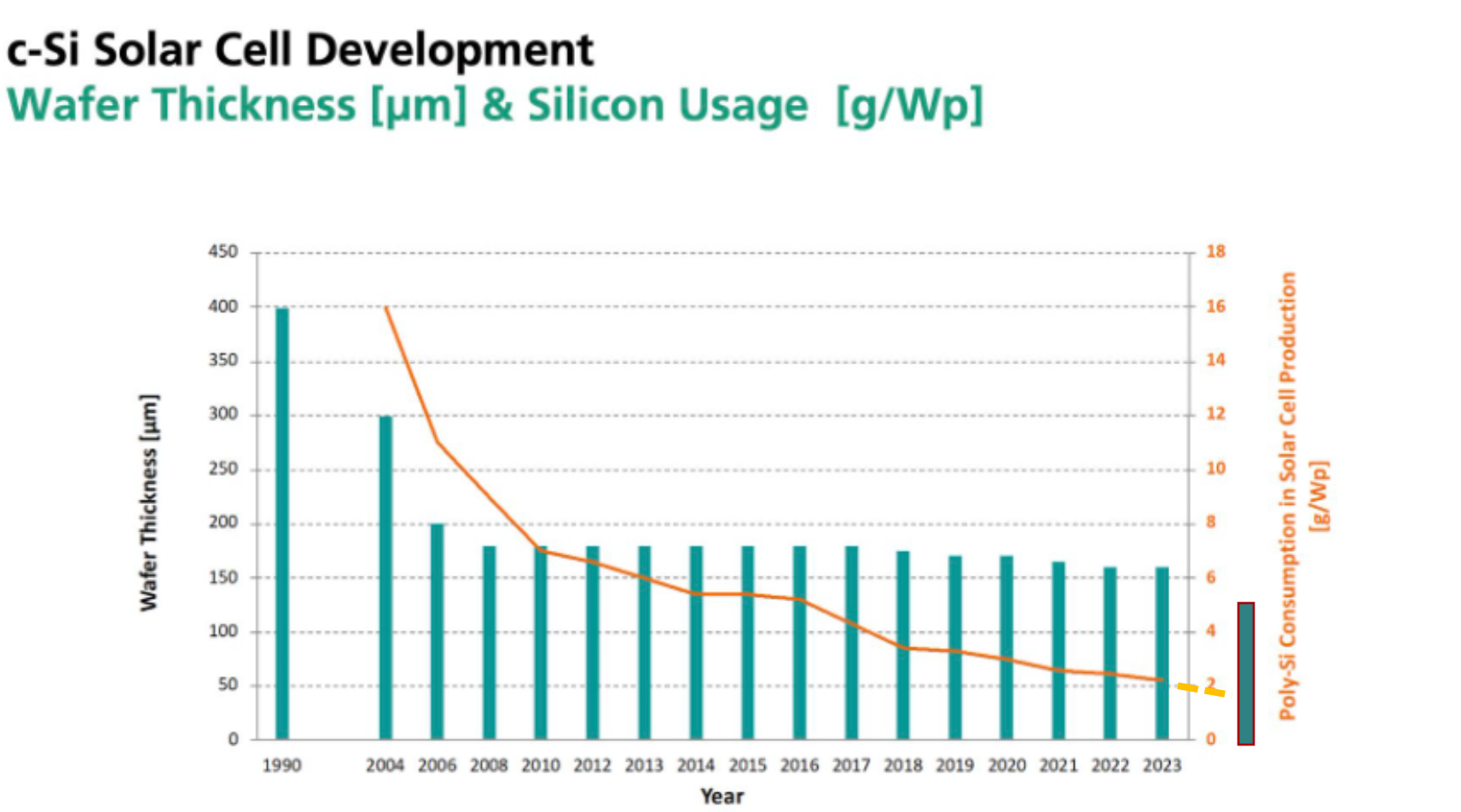
A note on Grey energy

Silicon usage per watt



Thinner wafers

Diamond Sawing

Efficiency

→

From 17 to 2 g/W in 20 years,

With low grey energy

Improved processes (Siemens)

Future: 1 TW PV per year → 2'000'000 tons of Si per year

A note on Grey energy of wafers and CO_2

Wafer «electricity cost» rough estimates

12 kWh/kg for MG si

50 kWh/kg for Siemens process and distillation

15 kWh/kg for pulling

4 kWh/kg for sawing

~ 90 kWh/kg electricity for from sand to wafers

If 500 W at 2 g/W → 0.18 kWh/W (around ½ of total modul)

A modern monocrystalline module
Needs ~ 0.4- 0.5 electrical kWh to produce (own estimates) in 2025

At 10 cts/kWh electricity, cost of electricity to make Si wafers 1.8 cts/W.

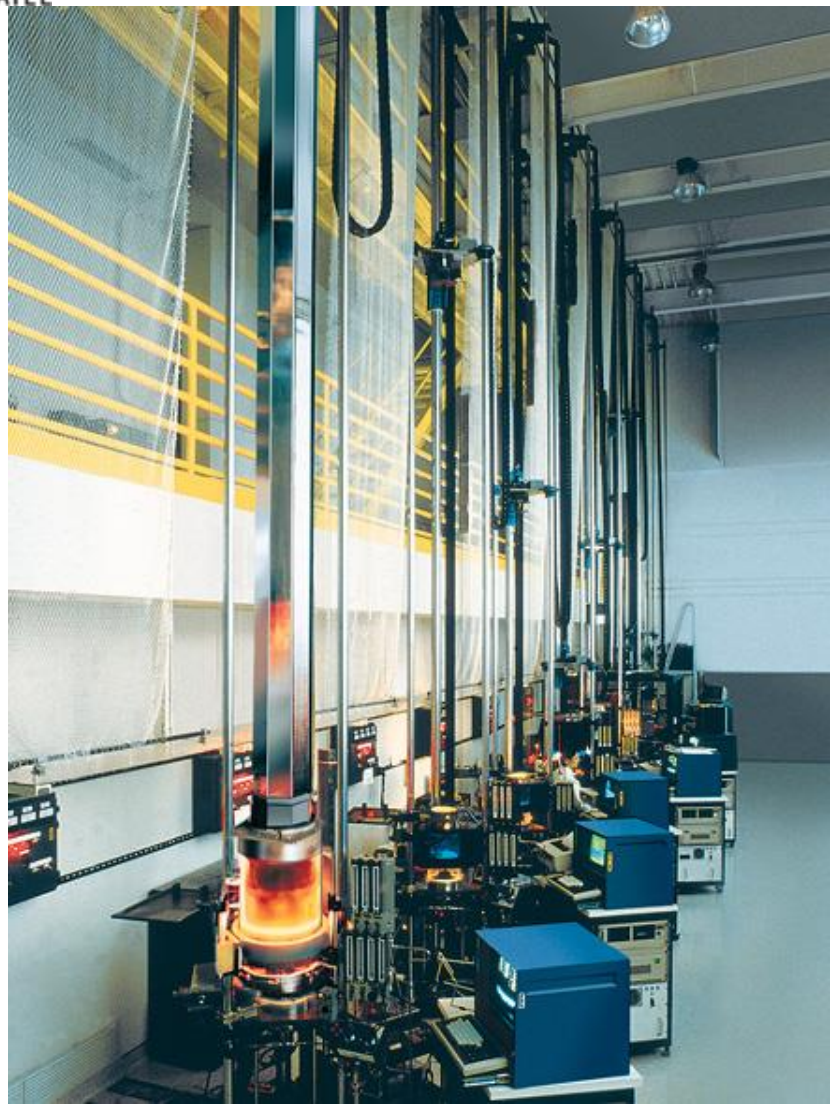
With proprietary coal powerplant at 5 cts/kWh → 0.9 cts/W

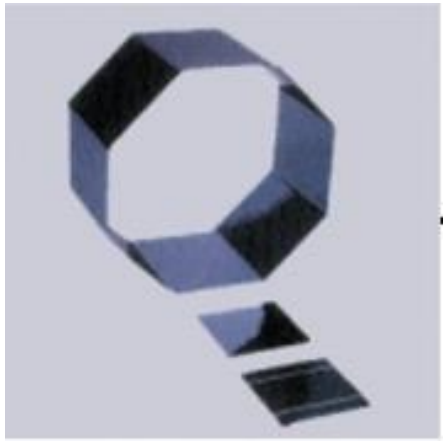
Many companies in Xianjiang use coal powerplants to produce polysilicon !

Not ideal
Wafer would accounts for ~ 180 g CO2 per Watt of modules if made only with coal electricity

Over 25 years 7gCO2 per kWh at wafer level

9. Alternative wafer preparation techniques





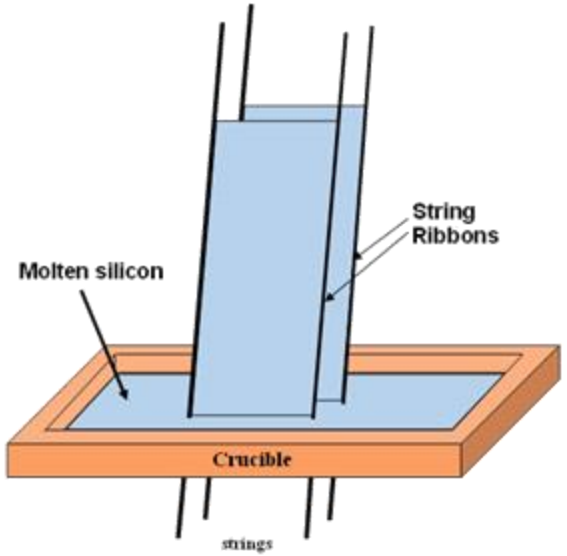
Edge defined Film fed growth from Schott (EFG) saves kerf losses, but they are still ~280 µm

By capillary action, the liquid silicon moves upward in a die. For a single die, growth is initiated at the edges of the die - which gave the name to this method.

~30 MW in 2008, discontinued now

9. Alternative wafer preparation techniques

String ribbon (SR) from Evergreen solar (Sovello) → save kerf losses



Heat-resistant wires are pulled vertically through a silicon melt, and the molten silicon spans and solidifies between the strings.

~ 80-150 MW
In 2012 at Sovello
Now stopped

9. Alternative wafer preparation techniques

Prof. Christophe Ballif

Startups with new wafering approach

1366

- Direct crystallization on a substrate from molten silicon
- Ramping up production line for wafers
- 19.6% cells proven together with Hanwha Q-cells early 2017!

9. Alternative wafer preparation techniques

Startups with new wafering approach

NEXWAFE

A start-up in Freiburg: Nexwafe

The NexWafe Wafer

The finished product – ultra thin, highly efficient drop-in replacements for conventional 120-140 µm wafers, produced with for 50% less cost and with a 75% reduction in CO2 emissions.

«Epitaxial wafer»

- Porous Si/anneal
- CVD growth
- Detaching

- Reuse of seed wafer

- Potential low wafer cost
- > 23% demonstrated (with heterojunction) by Crystal solar
- 28.9% tandem Perovskite/Si with CSEM **

(**Nexwafe and CSEM develop tandem perovskite 2-junction cells with 28.9% efficiency | Perovskite-Info

Alternative techniques

- Need to be further explored, would be still a high material/energy cost saving (at least in theory)
- In general: Not easy for any new wafering technology to compete in quality with Cz wafers and in cost, considering permanent improvements in pulling and sawing

Key take home messages/ to remember

- The general process from sand to modules, including the reactions for transforming silicon to a pure silicon, and the siemens process
- The typical level of acceptable impurities in polysilicon and why
- The various ingot growth methods (mono, multi, hp multi,quasi-mono,)
- Generalities about multi-wire sawing, with the transition to diamond wire sawing and the reduction of kerf loss down to 50 microns.
- Understanding the impact of cracks and fracture toughness on the strength of wafers, typically in the 150-500 MPa range.
- Orders of magnitude: in 2025: much lower Poly-Si 5 $/kg (down from 40 $/kg). Wafers 3 cts/W (China). Si usage 2 g/W of Si.
- Energy consideration: how much energy (roughly) and improvements to making polysilicon. rough estimates of 90 kWh/kg of sawn silicon grey energy for all steps from “sand” to wafer.
- Impact of efficiency, sawing, and polysilicon energy reduction on various LCA aspects !
- Some industry trends: go to larger wafer size (more productivity for wafers and cells, larger modules, switch from B to Ga doped wafers (because of B-O is not more considered), n-type doping with Antimony
- Monocrystalline n-type wafers dominate the market now. With high purity starting material, and clean crucible → possibible lifetime >> 1 ms for 2-3 Ohm cm material …

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